MASSACHVSETTS INSTITVTE OF TECHNOLOGY
Department of Electrical Engineering and Computer Science

6.002ex – Circuits and Electronics
Spring 2004

Problem Set 6
Readings and exercises for March 15 through March 28

Issued: 15 March 2004

Reading: Be sure to do the required readings *before class*

- Before lecture on March 29 read Agarwal and Lang, Chapter 9 and chapter 10, through section 10.4.

Since many students may not have access to the Web over spring break, the second part of this problem set does not use the on-line homework system. Have a great spring break!

Due Date Schedule for Radio Lab

By now, you have all finished building and testing the audio amplifier stage of your radios. Over the next few weeks, you should all finish the complete radio. We'll try to provide help in the lab on Fridays, but you can work with your partner in the lab whenever the lab is open by checking out one of the soldering irons we've provided for 6.002x. Please work in the lab *together with your partner*—don't just divide the work up and each do parts of the work alone. Feel free to ask us to schedule times to meet you for help if you get stuck.

Although you can work on this at your own times over the coming weeks, you'll be required to finish parts of the radio according to a definite schedule. Make sure to do the various tests at the end of each construction phase. These are important not only for understanding what is going on, but also for making sure that things are working before you go on to the next step. We'll be checking over the coming weeks to make sure that you are keeping up with the schedule. You're encouraged to work more quickly than this schedule, but you must finish each part by the date indiated. Assume that each of the parts here will take you about as much time to build as did the audio amplifier.

Part	through page	completed by
Audio Preamp	35	April 2
Local Oscillator	41	April 2
RF Amplifier/Mixer/Converter	48	April 9
Detector	51	April 16
First IF Amplifier	56	April 23
Second IF Amplifier	62	April 30
Detector and AGC	64	April 30

Part 1: To do on line before recitation on Friday, March 19

1.1: Static Discipline Suppose we have a logic family for which $V_{DD} = 5$ Volts and the static discipline is $V_{OH} = 4.5$ Volts, $V_{IH} = 4$ Volts, $V_{IL} = 1.5$ Volts, and $V_{OL} = 1$ Volt. What are the low and high noise margins for this family? What is the width of the forbidden region?

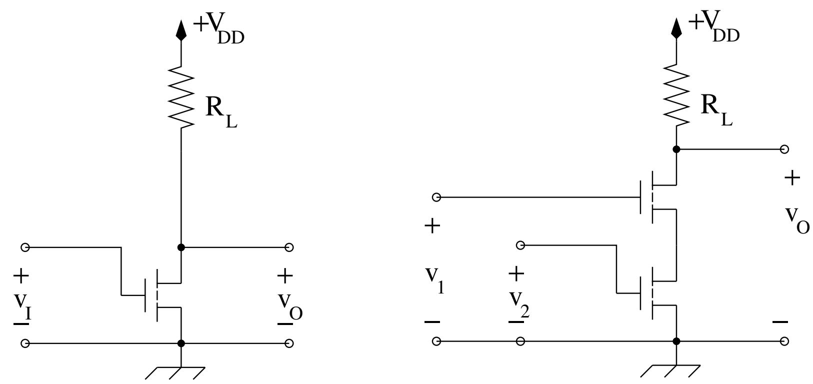

Figure 1: An inverter and a NAND gate implemented using FETs

1.2: MOSFET Gates

1. For many purposes of gate design, we can model a MOSFET used as a switch simply as as an ideal switch and an "on-state resistor" resistor R_{ON}. This is the SR model discussed in Agarwal and Lang, section 6.6.

   Suppose that the threshold voltage V_T for the MOSFET is 2.0 Volts and R_{ON} is a value that you will given in the on-line homework system.

   Assuming this model for the MOSFET, consider the inverter in figure 1(a). This inverter is intended to be used as an element in the logic family described above in part 1.1 above. What is the minimum value of the pullup resistor R_L for which this inverter can obey the required static discipline?

2. We'd like to use these same MOSFETs to implement, for the same logic family, the NAND gate shown in figure 1(b). Now what is the minimum value of R_L for which this gate can obey the required static discipline? Assume the same parameters as in part (1).

3. Suppose we've implemented the NAND gate with R_L the minimum value you found in part (2). For what values of the inputs (LOW or HIGH) does the gate consume maximum power? What is this maximum power?

Part 2: To write up and turn in at lecture on Monday, March 29

2.1: First-order transients Do exercise 19 in chapter 10 of Agarwal and Lang. For each circuit, in addition to choosing the matching graph, derive the differential equation for v_O in terms of R, C, and v_S, and solve the equation.

2.2: Propagation delay in MOSFET gates Read section 10.4 of Agarwal and Lang, paying special attention to section 10.4.2, which shows that the propagation delay for a certain inverter is $t_{pd} = 0.2$ ns (actually, they get $t_{pd} = 0.1928$ ns, but that seems overly precise). For the example in the book, the pullup resistor is $R_{\mathrm{L}} = 10\ \mathrm{K}\Omega$. Redo the computations in this example, assuming that $R_{\mathrm{L}} = 15\ \mathrm{K}\Omega$, to show how this affects the propagation delay for high-to-low and low-to-high transitions. Don't just write down the answer—repeat the derivation in the book, showing how the values change at each step.

2.3: Response to a ramp input Section 10.1.1 of the book shows that the capacitor voltage response of a parallel RC circuit to a step in current

$$i(t) = I_0 \qquad t > 0$$

is

$$v_C = I_0 R \left(1 - e^{-t/RC}\right)$$

Compute the analogous response of this same circuit to a *ramp* in current

$$i(t) = I_0 t \qquad t > 0$$

Be sure to show all your work.

Hint: If you are looking for a particular solution to an equation of the form

$$A\frac{dx}{dt} + Bx = Ct$$

try solutions of the form $x(t) = \alpha t + \beta$.