MASSACHVSETTS INSTITVTE OF TECHNOLOGY
Department of Electrical Engineering and Computer Science

6.002x – Circuits and Electronics
Spring 2004

Problem Set 5

Issued: 1 March 2004

Quiz 1 will be on Friday, March 5 in your recitation section. The quiz will be closed book, except for one additional page of notes that you may have prepared. You may bring a calculator to the quiz if you wish, but it should not be necessary.

Reading: Be sure to do the required readings *before class* as indicated.

- Before lecture on Monday, March 8, read Sections 6.7 (page 424), 7.1–7.5 (pages 467–494) from Agarwal and Lang.
- Before lecture on Wednesday, March 10, read the following parts of Agarwal and Lang on Digital Abstraction: Sections 5.1, 5.2, 5.3. (pages 351–377).
- The rest of chapters 6 and 7 are available for your reference. All the material that you need to know about transistors and amplification will be presented in lecture and in handouts.
- Before lecture on Monday, March 15, read parts of chapter 9: sections 9.1, 9.2 (pages 613–631).

Note: The first part of this problem set continues the study of the simple common-emitter amplifier that you analyzed in problem set 4. In this problem set your job is to synthesize a common-emitter amplifier to meet a required specification. You will do this synthesis online, using some new software, so we will appreciate bug reports. There are also two questions to write up and turn in.

The second part of the problem set deals with models for MOS transistors. You should write this up and turn it in.

The amplifier synthesis problem

You'll be working with the same common-emitter amplifier as last week, shown in figure 1, and you'll do the design problem in three phases:

1. Determine values for the resistors to obtain bias conditions that satisfy the swing and gain specifications, given the power supply voltage. In this phase of the design, we assume that β of the transistor is infinite and that the approximate gain of the stage is the ratio $v_o/v_i = -R_{\mathrm{C}}/R_{\mathrm{E}}$. (You should have discovered this in problem set 4!)

2. Abandon the $v_o/v_i = -R_{\mathrm{C}}/R_{\mathrm{E}}$ assumption, but retain the $\beta = \infty$ assumption for bias conditions. Now, the gain is determined by the incremental model. Here you must adjust your choices so that the input impedance of your amplifier stage exceeds the required minimum input impedance.

3. Now abandon the $\beta = \infty$ assumption. This may require further changes to meet all the specifications.

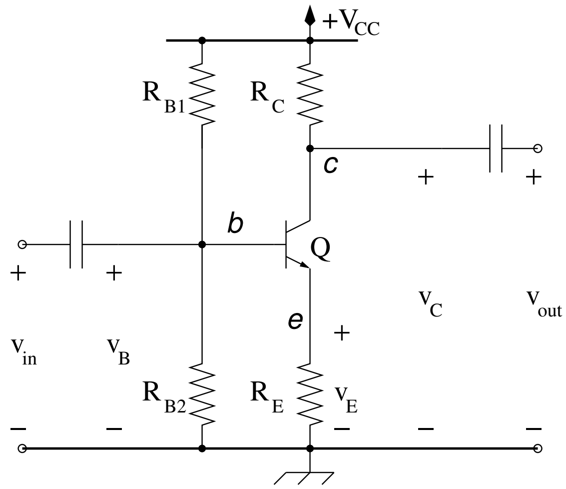


Figure 1: An essential transistor amplifier circuit: the common-emitter amplifier.

Experienced designers don't attack a synthesis problem like this by simply guessing values for the resistors. Rather, they make assumptions about reasonable operating conditions and reason backwards from these to determine what the resistor values must be.

The on-line system you will be working with permits you to assume values for whichever of the unknowns you wish, in any order you wish. When you specify a value for an unknown, the system will use its knowledge of circuit theory to deduce the consequences of setting that value. For example, if there is a node with three currents entering it, and you assume values for two of the currents, the system will use KCL to deduce the value of the third current.

Another possible consequence of assuming a value may be that it contradicts some known condition. For example, too small a voltage from the collector to the emitter of the transistor will contradict the assumption that the transistor is operating in the amplifying region. The system will signal these contradictions and give you an opportunity to remove a previous assumption. [1]

Problem 1.1: Crude Bias Synthesis – To do on line and to write up and hand by lecture on Monday, March 8

Good designers know that one should attack the hardest part of the design first. In this case one should try to choose the collector bias voltage.

The nasty part of choosing the collector bias voltage is the swing specification. The swing specification describes a required range for the collector voltage. For example, if the swing specification is 6 Volts then the collector voltage must be able to rise to 6 Volts above the collector-voltage bias point and it must be able to fall to 6 Volts below the bias point. Sounds easy, but there is a

[1] The program you are using includes an electrical circuit simulator, a constraint propagator, and a truth maintenance system. You should be impressed. You learned about constraint propagation in 6.001, and you can learn about how truth maintenance in 6.034.

This is also *very* experimental software, so don't be surprised if you fund problems. Even better, suggest ways that you'd like to see this improved. If you are interested, there might be some UROP slots for working on this.

complication: as the collector falls the emitter rises, but the collector voltage must remain above the emitter voltage for the transistor to remain in the amplifying region.

Once the collector bias voltage is known, it is prudent to pick the collector bias current. This will determine lots of things. Most small-signal transistors prefer bias currents within a factor of 10 of 1mA. This is usually determined by how much power you want to dissipate in the transistor (and how hot it is allowed to get.)

Use the online system to go through the Crude Bias Synthesis Phase. The system will assign you a specification to meet. Each person will get a different specification.

After you have completed this phase and obtained an acceptable set of values for the resistances, we want you to reflect on the experience. Write up an answer to the following questions, to be handed in.

- The power-supply voltage, the gain, the collector-bias voltage, and the collector-bias current determine the emitter resistance. Show that

$$R_{\mathrm{E}} = \frac{V_{\mathrm{CC}} - V_{\mathrm{C}}}{|g| I_{\mathrm{C}}},$$

  where V_{CC} is the power-supply voltage, V_{C} is the collector-bias voltage, I_{C} is the collector-bias current, and $|g|$ is the absolute value of the gain.

- The power-supply voltage, the gain, and the swing specification constrain possible values of the collector-bias voltage. Show that

$$\frac{V_{\mathrm{CC}} + (|g|+1)\Delta v_{\mathrm{C}} + V_{\mathrm{SO}}|g|}{|g|+1} < V_{\mathrm{C}} < V_{\mathrm{CC}} - \Delta v_{\mathrm{C}},$$

  where Δv_{C} is the required swing (up or down), and $V_{\mathrm{SO}} \approx 0.2$ Volts is the minimum voltage from the collector to the emitter that allows amplification.

Problem 1.2: Incremental Synthesis – To do on line and to write up and hand by lecture on Wednesday, March 10

We now assume that the bias points that you have chosen with the infinite β assumption are appropriate. Using these we consider the incremental behavior of the circuit. Here the simple assumption that $v_o/v_i = -R_{\mathrm{C}}/R_{\mathrm{E}}$ is not true. The bias current into the collector of the transistor determines the transconductance and the small-signal input resistance (using $\beta \approx 100$ and the relation $g_m r_\pi = \beta$).

This changed assumption will change some of the values derived from your choices in the crude bias synthesis. Your design now needs to meet an additional constraint, that the input impedance of the amplifier is big enough. At first blush it might appear that the input impedance is just the parallel combination of the base-bias resistors R_{B1} and R_{B2}, but the incremental model allows some incremental current to enter the base of the transistor through r_π. Thus the input impedance will be smaller than this parallel combination, and it will depend on the collector bias current that you have previously chosen.

Use the online system to do the Incremental Synthesis.

Warning: Do not go back and restart the bias synthesis or else your bias assumptions will be lost. If you wish to change those assumptions you may do so from the incremental synthesis page.

After you have completed this phase and obtained an acceptable set of values for the resistances, we want you to reflect on the experience. Write up an answer to the following question, to be handed in.

- Show that the incremental input impedance of the amplifier is the parallel combination of the two base bias resistors and a quantity that is inversely proportional to the collector-bias current.

Problem 1.3: Finite Beta Synthesis – To do on line before lecture on Monday, March 15

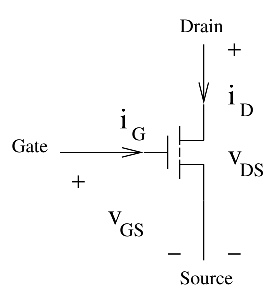
Of course, the β of the transistor is not infinite, so the bias points you have chosen may really depend on the resistances of the base-bias resistors: The small bias current into the base of the transistor changes the voltage on the base, thus changing the emitter voltage, and thus, perhaps the collector current! It is important to check your results by accounting for this current. If you are lucky the values you have already chosen will work when the β is assumed finite. If not, you will have to make some (hopefully small) adjustments.

Use the online system to complete the Finite Beta Synthesis.

Warning: Do not go back and restart the bias synthesis or the incremental synthesis, or else your previous assumptions will be lost. If you wish to change those assumptions you may do so from the Finite Beta Synthesis page.

2.1: To write up and turn in at Lecture on Monday, March 15.

We introduce MOSFETs (*M*etal-*O*xide-*S*emiconductor *F*ield-*E*ffect *T*ransistors) in lecture on March 8. The schematic symbol for an NMOS transistor is shown below, labeled with its circuit variables. (There is also a complementary PMOS transistor, as with BJTs.)



The behavior of the NMOS transistor depends upon two parameters, K and V_T. Typical values are $K = 2$ mA Volt^{-2} and $V_T = 2$ Volts. The behavior is summarized in the following formulas:

$$i_G = 0$$

$$
i_{\mathrm{D}} = \begin{cases} 0 & \text{if } v_{\mathrm{GS}} - V_{\mathrm{T}} < 0 & \text{(cutoff)} \\ \frac{K}{2}(v_{\mathrm{GS}} - V_{\mathrm{T}})^2 & \text{if } 0 < v_{\mathrm{GS}} - V_{\mathrm{T}} < v_{\mathrm{DS}} & \text{(amplification)} \\ K\left((v_{\mathrm{GS}} - V_{\mathrm{T}})v_{\mathrm{DS}} - \frac{v_{\mathrm{DS}}^2}{2}\right) & \text{if } 0 < v_{\mathrm{DS}} < v_{\mathrm{GS}} - V_{\mathrm{T}} & \text{(switched on)} \end{cases}
$$

1. If the MOSFET is switched on, what is the incremental drain-source resistance ($v_{\mathrm{ds}}/i_{\mathrm{d}}$) when $V_{\mathrm{DS}} = 0$? What this value when $V_{\mathrm{GS}} = 2.5$ Volts?

2. What is the incremental transconductance, i.e., the ratio of the incremental drain current to the incremental gate-source voltage ($i_{\mathrm{d}}/v_{\mathrm{gs}}$) for a MOSFET biased into the amplification region? (Your answer should express the transconductance as a function of the parameters K and V_{T} and the bias voltage V_{GS}.) What is this value for $V_{\mathrm{GS}} = 2.5$ Volts, $V_{\mathrm{T}} = 2$ Volts, and $K = 2$ mA Volt^{-2}?

   As we have seen, the analogous relation for a BJT is the relation between the emitter current i_{E} and the base-emitter voltage v_{BE}. Show that for a BJT, the incremental transconductance is approximately proportional to the emitter current I_{E}, while for a MOSFET, the incremental transconductance is proportional to the square root of the drain current I_{D}.