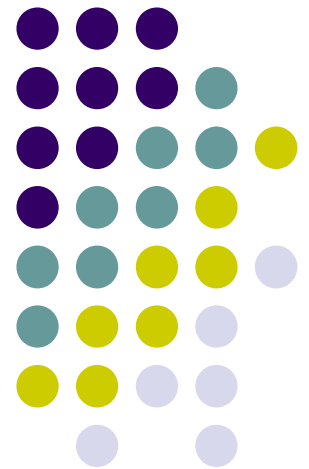


# FAST: FPGA Acceleration for SimulaTors

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# What?

- Accelerate cycle-accurate simulators using FPGAs
  - Conventional processors
  - Network processors
  - CMPs
- Goal is 3 to 4 orders of magnitude performance improvement
  - Ones to tens of millions of instructions per second
- Ability to study “real” applications running on top of a real operating system and generate highly accurate microarchitecture performance predictions

# Current Cycle-Accurate simulators

UT FAST

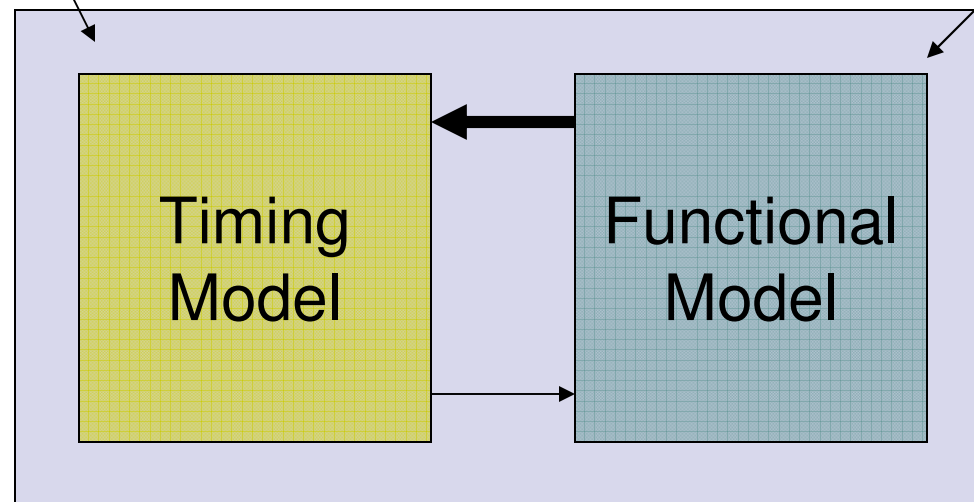
Who  
What  
How  
Why

- Microarchitecture
- Resource contention
- dependencies

*1K-10K  
inst/sec*

- ISA
- I/O devices

Run on PC



Generally incapable of running unmodified OS???

*Simplescalar  
SimOS*

*DEC/Compaq/Intel ASim*

# FAST Philosophy

- “You’ve got lots of tools and not everything is a nail”
- Most ISAs have sequential semantics
  - Simulate in software (that has sequential semantics)
  - Processors have the hardware to execute instructions (floating point, etc.)
- Microarchitecture has parallel semantics
  - Simulate in hardware to express concurrency (much faster)
  - Much simpler (e.g., associative cache)
  - Stats do not slow down simulation (up to a certain point)
- *Let functional model do the heavy ISA lifting*
  - Instruction decode, execution, ISA state maintenance
  - Accurate enough to run unmodified applications and OSs at reasonable speeds
- Timing model does not model ISA only resource contention & constraints!
  - E.g., cache tags only, no ALU operations, etc.

# FAST

UT FAST

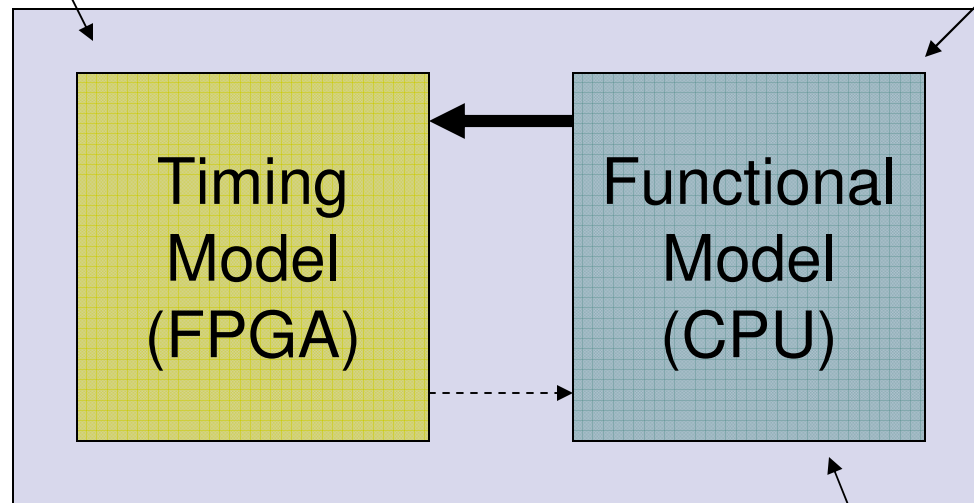
Who  
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*1M-100M  
Inst/sec*

- ISA
- I/O devices

Pure FPGA or  
FPGA+computer



Capable of running unmodified OSs  
10M-100M inst/sec

*BOCHS  
SimICS*

# Why?

- Simulator speed is becoming important
  - Complexity
    - Systems
    - Applications
  - Range
    - Can explore many more options
  - Numbers
    - CMPs/Network processors
- Completeness
  - Makes full-system simulation cycle-accurate
  - OS can take more than 50% of CPU cycles, must have *some* performance impact