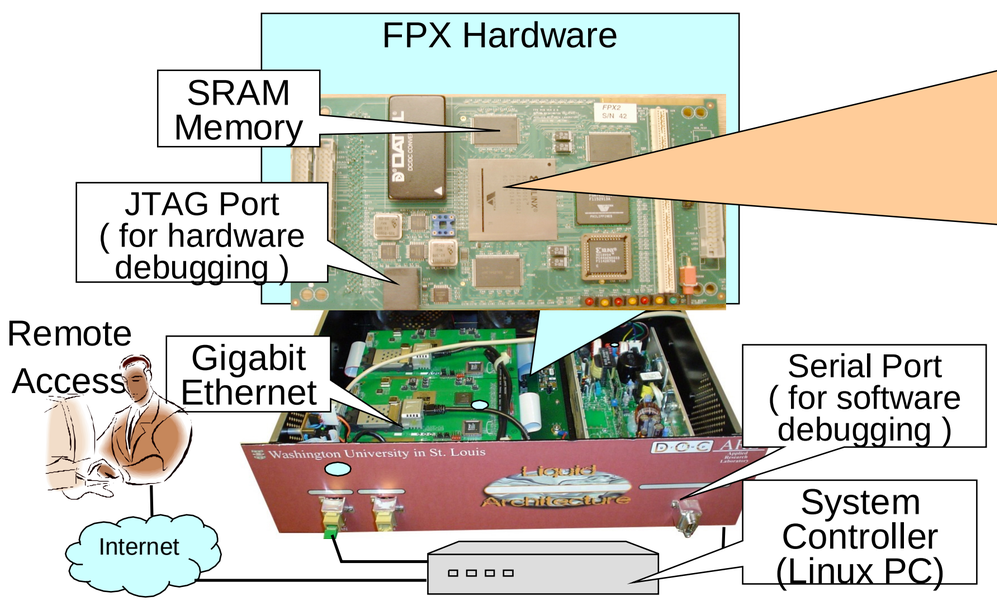
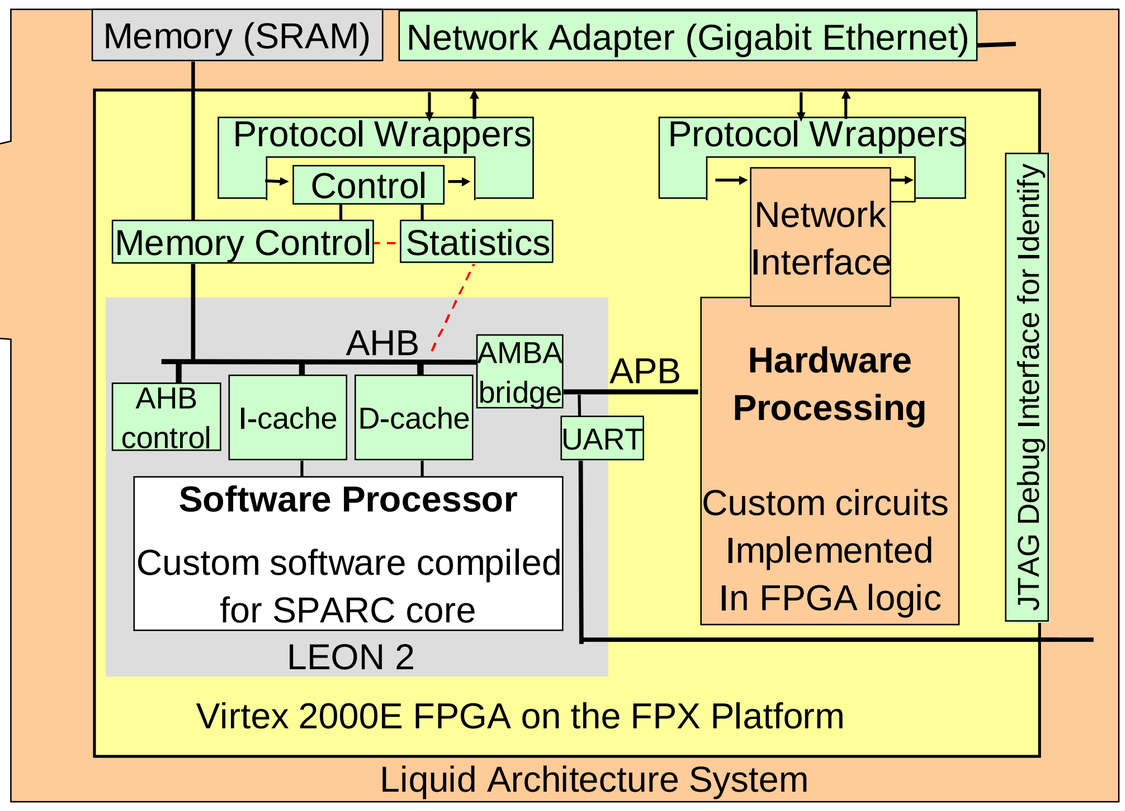
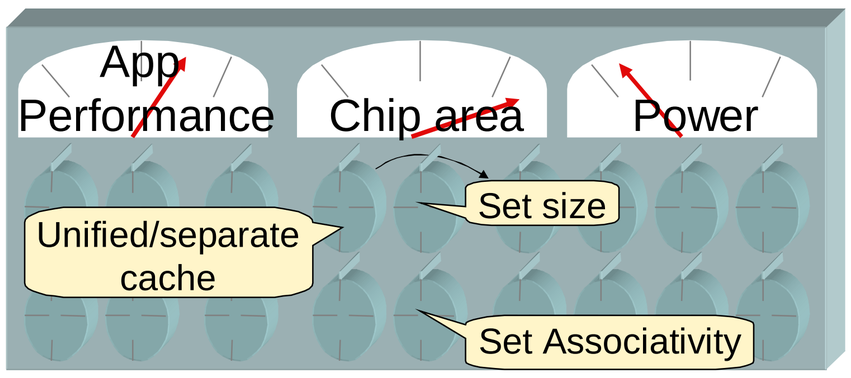
Semi-Automatic Microarchitecture Configuration of Soft-Core Systems

by Shobana Padmanabhan

The platform:







~48 reconfigurable parameters for LEON

Better than existing approaches which

- *Simulate all configurations exhaustively*
- *Consider only some of the tunable parameters*
- *Not feasible to simulate applications with long runtimes*

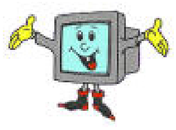
Tuning

Manual
Requires expert architect & application knowledge

Automatic

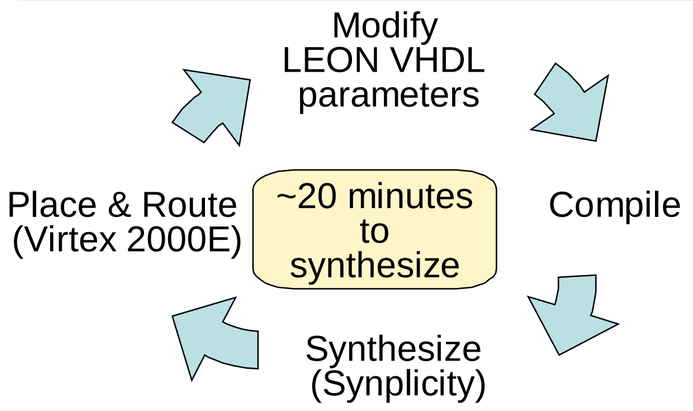
Exhaustive

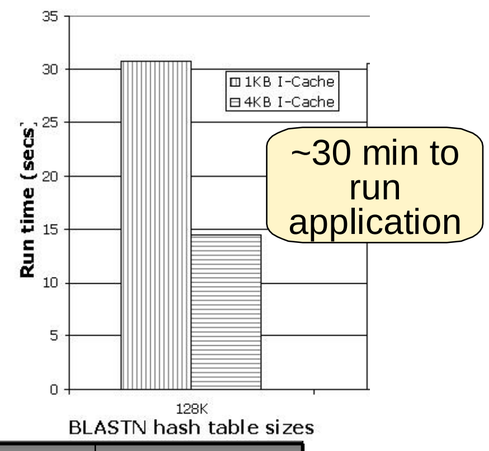
Heuristic



Architect expertise & Application knowledge helps but not mandatory..

Optimization challenges: Expensive data-points





Yes/No	Variable	Area Incr %	Time Dcr%
iCache setsize=1KB	CS_1	4	0
iCache setsize=2KB	CS_2	7	10
iCache setsize=4KB	CS_3	20	50
…	…	…	…
iCache setsize=64KB	CS_7	80	51
iCache assoc=1way	CA_1	5	0
iCache assoc=2way	CA_2	7	1
iCache assoc=3way	CA_3	10	1
iCache assoc=4way	CA_4	20	1
dCache setsize=1KB	DS_1	3	0
dCache setsize=2KB	DS_2	5	1
…	...	…	…

Approach

Identify independent parameters

Generate data points

Generate Integer Programming for optimal configuration

Store for future reference

BINARY VARIABLES
$CS_1, CS_2, CS_3,\ldots, CS_7, CA_1, CA_2, CA_3, CA_4,$
$DS_1, DS_2, DS_3,\ldots, DS_7, DA_1, DA_2, DA_3, DA_4,\ldots$

MINIMIZE
$Z = .5(\ 4CS_1 + 7CS_2 + 20CS_3 + \ldots + 80CS_7 +$
$5CA_1 + 7CA_2 + 10CA_3 + 20CA_4 +$
$3DS_1 + 5DS_2 + \ldots) +$
$.5(\ 0CS_1 - 10CS_2 - 50CS_3 - \ldots - 51CS_7 -$
$0CA_1 - 1CA_2 - 1CA_3 - 1CA_4 -$
$0DS_1 - 1DS_2 - \ldots)\ ;$

weight for 'area'

weight for 'runtime'

SUBJECT TO
$4CS_1 + 7CS_2 + 20CS_3 + \ldots + 80CS_7 +$
$5CA_1 + 7CA_2 + 10CA_3 + 20CA_4 +$
$3DS_1 + 5DS_2 + \ldots \quad <= 100;$

'area' constraint

$4CS_1 + 7CS_2 + 20CS_3 + \ldots + 80CS_7 \quad = 1;$
$5CA_1 + 7CA_2 + 10CA_3 + 20CA_4 \quad <= 1;$

'binary' constraints

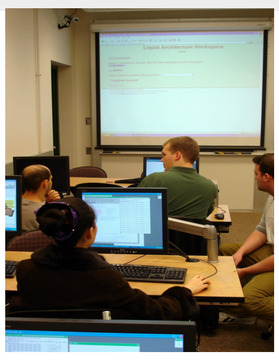
…

$CS_i >= 0,\ i = 1, 2, \ldots, 7 \quad CA_j >= 0,\ j = 1, 2, 3, 4 \ldots$

'non-negative' constraints

A typical Integer Programming model..

Platform also being used for teaching



Hardware/ software co-design
- New hardware hash instruction
- Network packet processing:
  Packet encoding/ decoding

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http://liquid.arl.wustl.edu
Funded by NSF under grant 03-13203