Reducing Instruction Cache Energy Using Gated Wordlines

by

Mukaya Panich

Submitted to the Department of Electrical Engineering and Computer Science
in Partial Fulfillment of the Requirements for the Degree of
Master of Engineering in Electrical Engineering and Computer Science
at the Massachusetts Institute of Technology

August 20, 1999

Copyright 1999 Mukaya Panich. All rights reserved.

The author hereby grants to M.I.T. permission to reproduce and distribute publicly paper and electronic copies of this thesis and to grant others the right to do so.

Author	
	Department of Electrical Engineering and Computer Science
	August 20, 1999
Certified by	
	Professor Krste Asanovic
	Thesis Supervisor
Accepted by	
•	Professor Arthur C. Smith
	Chairman, Department Committee on Graduate Theses