Reducing Instruction Cache Energy Using Gated Wordlines
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ABSTRACT

The power dissipated by the level-1 Instruction cache is often a considerable part of the total power dissipated by the entire microprocessor. In this thesis, we focuses on reducing the power consumption of the I-cache by using an in-cache instruction compression technique that uses gated wordlines to reduce the number of bitline swings. First, we develop a cache power consumption model to estimate the power dissipated in the I-cache. Next, we examine the effectiveness of two design techniques previously proposed to reduce power consumed in the I-cache; sub-banking and reducing the frequency of tag compare. We then investigate two versions of our technique that uses gated wordlines. The first version involves using instructions of one of two sizes, medium or long. The second version uses three instruction sizes, short, medium and long. We evaluate our technique by applying it to the MIPS-II instruction set. Our dynamic compression for programs in SPECInt95 achieves an average reduction in bits read out of 23.73% in the 2-size approach and 29.10% in the 3-size approach.

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