Symposium on VLSI Circuits 2002

Leakage-Biased Domino Circuits for Dynamic Fine-Grain Leakage Reduction

Seongmoo Heo and Krste Asanović

Massachusetts Institute of Technology
Lab for Computer Science

Leakage Power

- Growing impact of leakage power
  - Increase of leakage power due to scaling of transistor lengths and threshold voltages
  - Power budget limits use of fast leaky transistors
- Challenge:
  - How to maintain performance scaling in face of increasing leakage power?

Leakage Reduction Techniques

- **Static: Design-time Selection of Slow Transistors (SSST) for non-critical paths**
  - **Replace fast transistors with slow ones on non-critical paths**
  - **Tradeoff between delay and leakage power**
- **Dynamic: Run-time Deactivation of Fast Transistors (DDFT) for critical paths**
  - **DDFT switches critical path transistors between inactive and active modes**

Observation:

Critical paths dominate leakage after applying SSST techniques

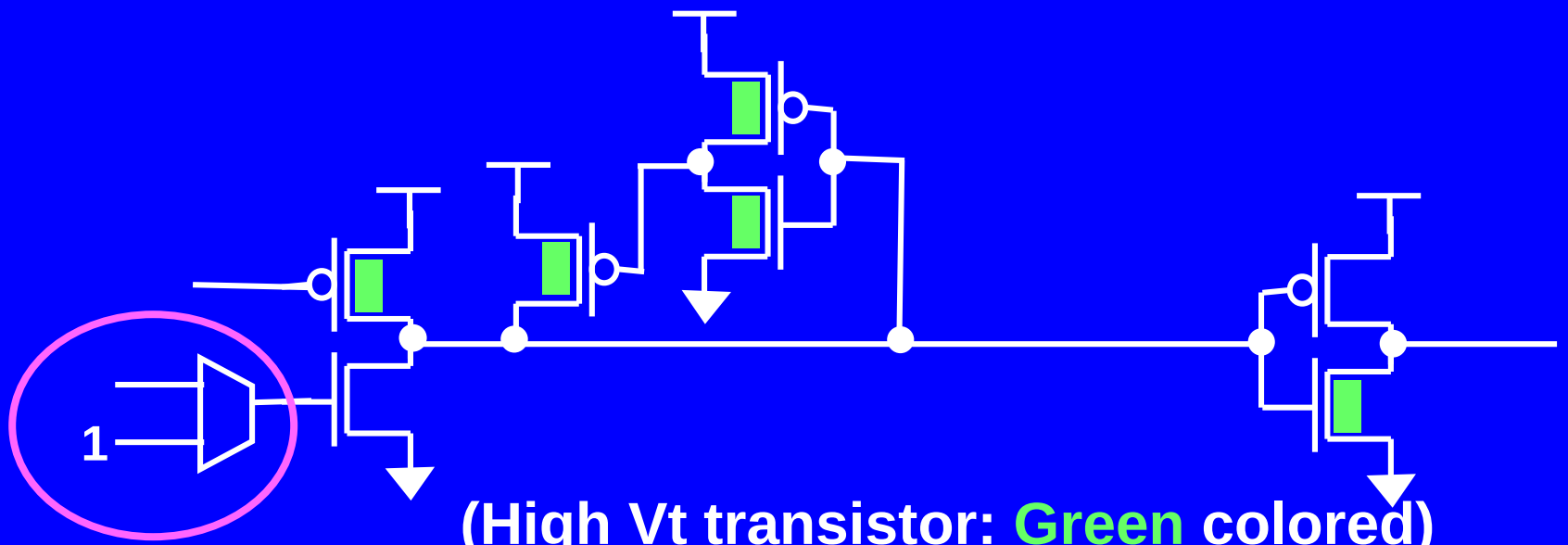
Example: PowerPC 750

- **5% of transistor width is low Vt, but these account for *>50%* of total leakage.**

⇒DDFT could give large leakage savings

DDFT Techniques for Domino

- **Dual-V_t Domino** ***[Kao and Chandrakasan, 2000]***
  - **High V_t for precharge phase**
  - **Input gating → increased delay and active energy**
  - **High Vt keeper → increased noise margin**



(High Vt transistor: Green colored)

DDFT Techniques for Domino

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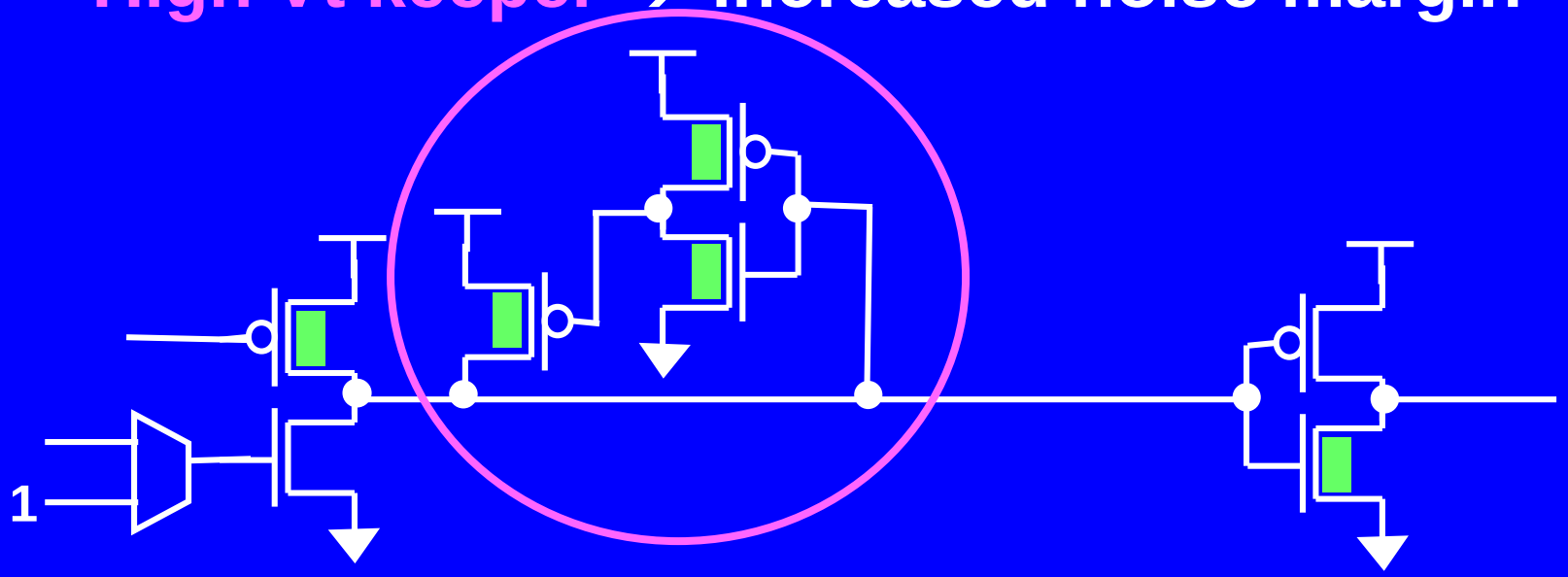
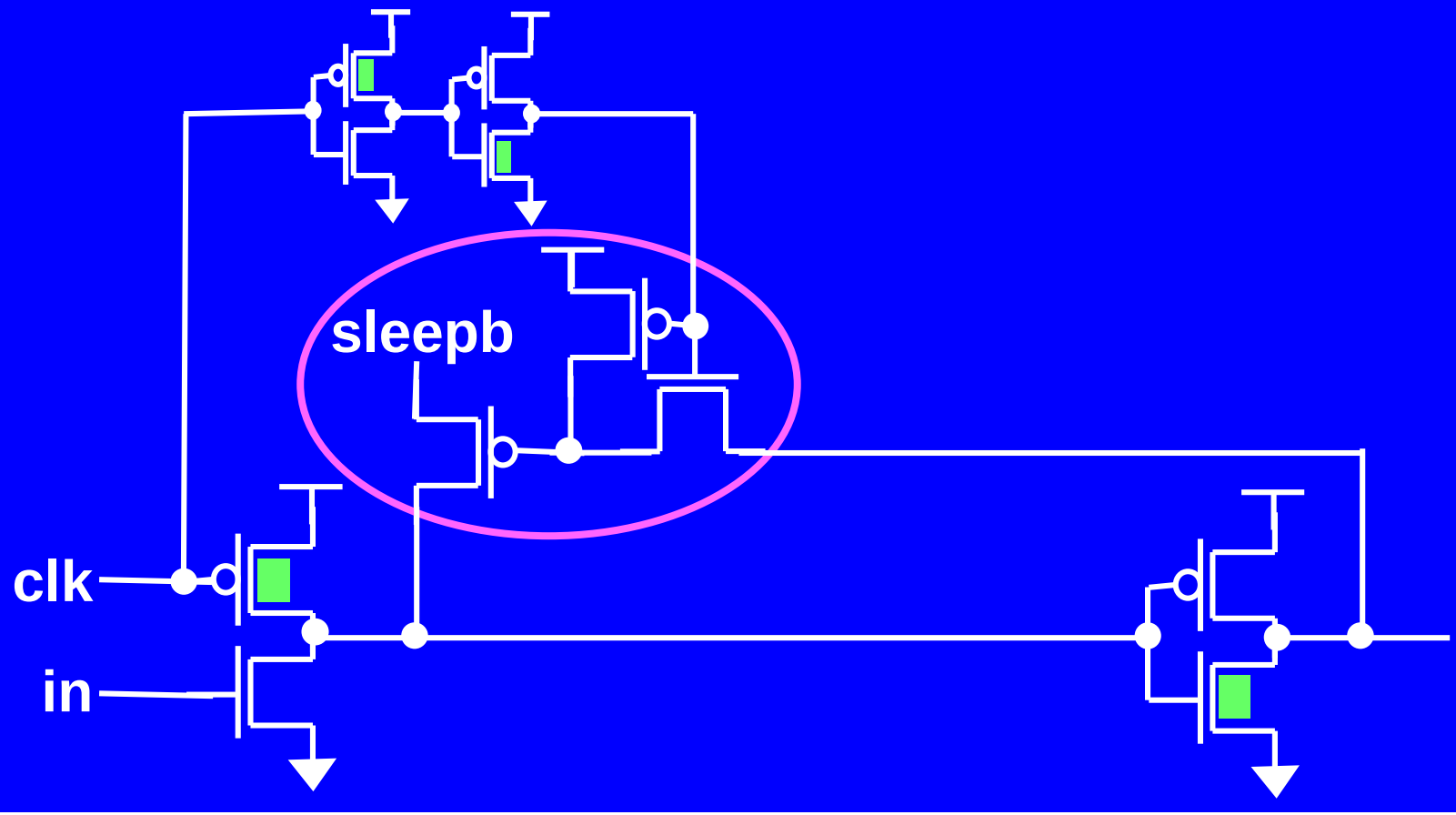


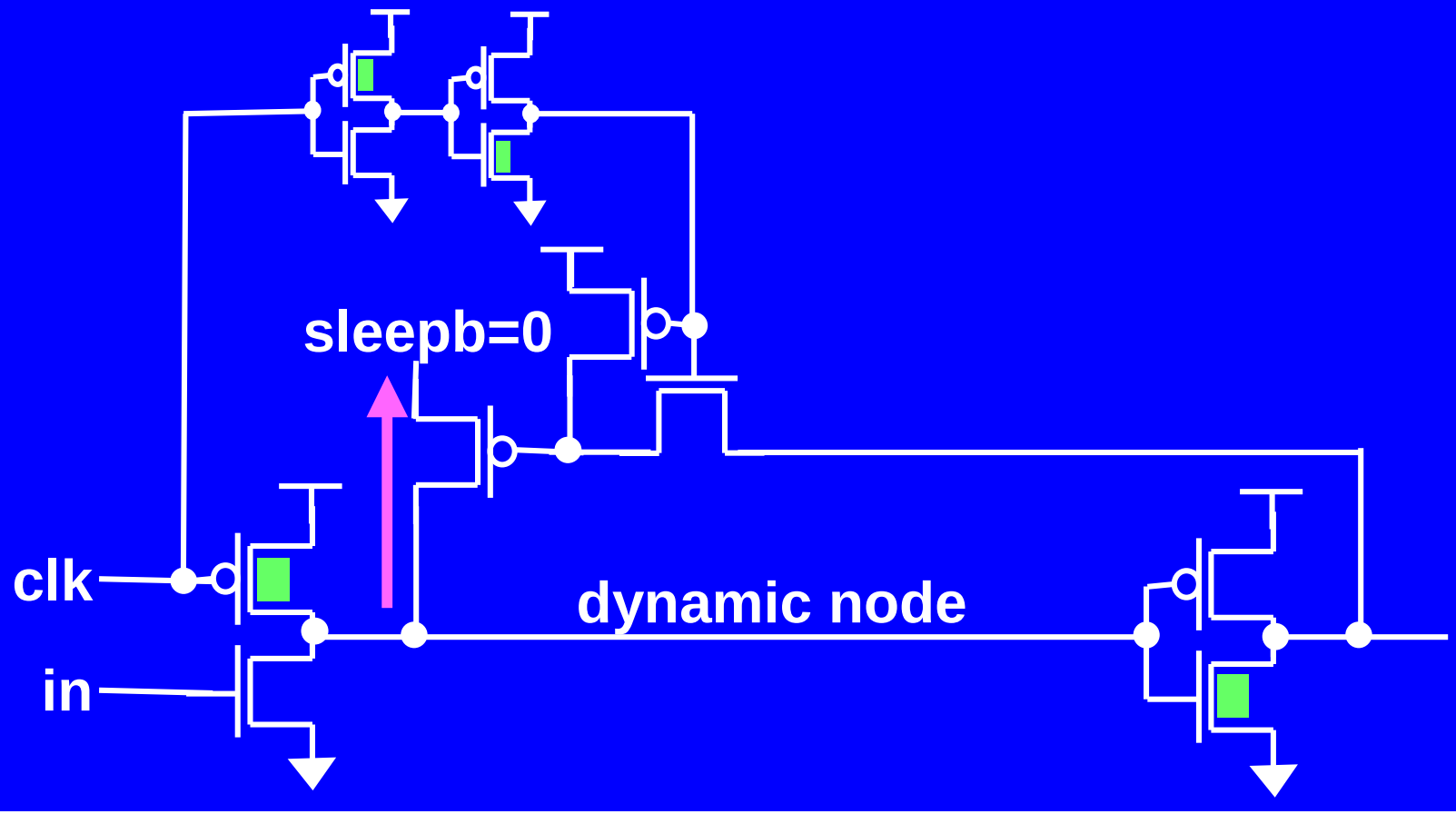
DDFT Techniques for Domino

- **MHS-Domino** ***[Allam, Anis, Elmasry, 2000]***
  - **Clock-delayed keeper**

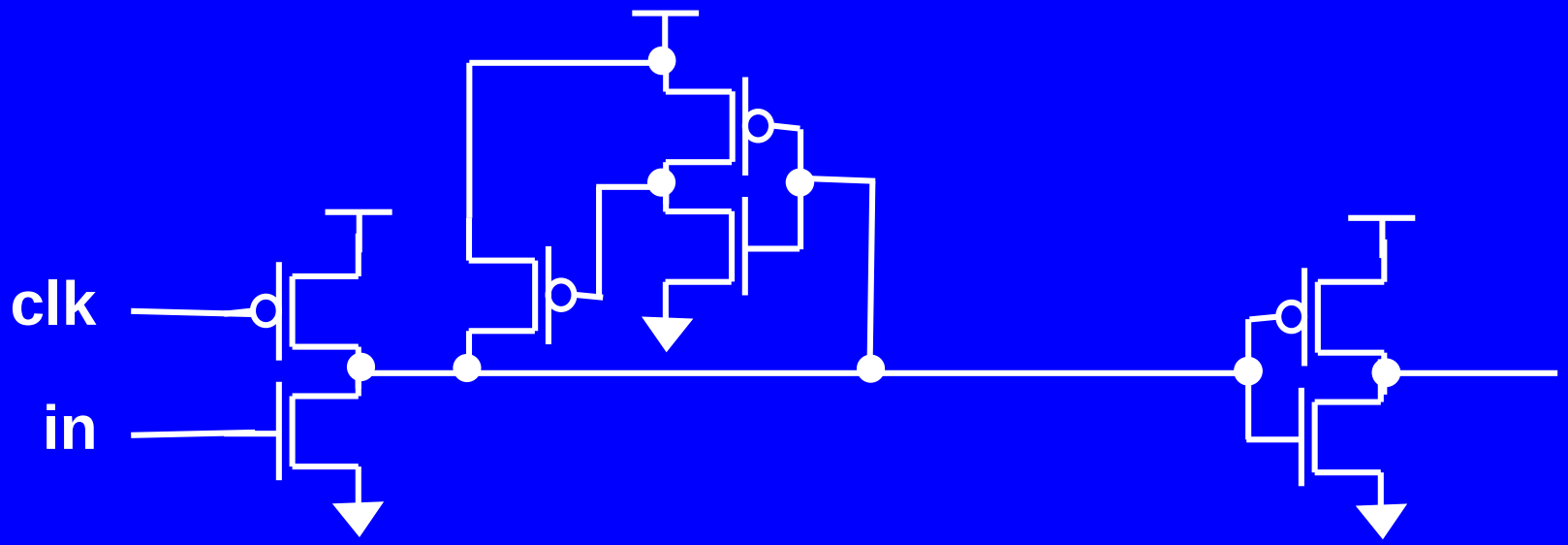


DDFT Techniques for Domino

- **MHS-Domino**
  - **Pull-down through PMOS → short circuit-current in static inverter**

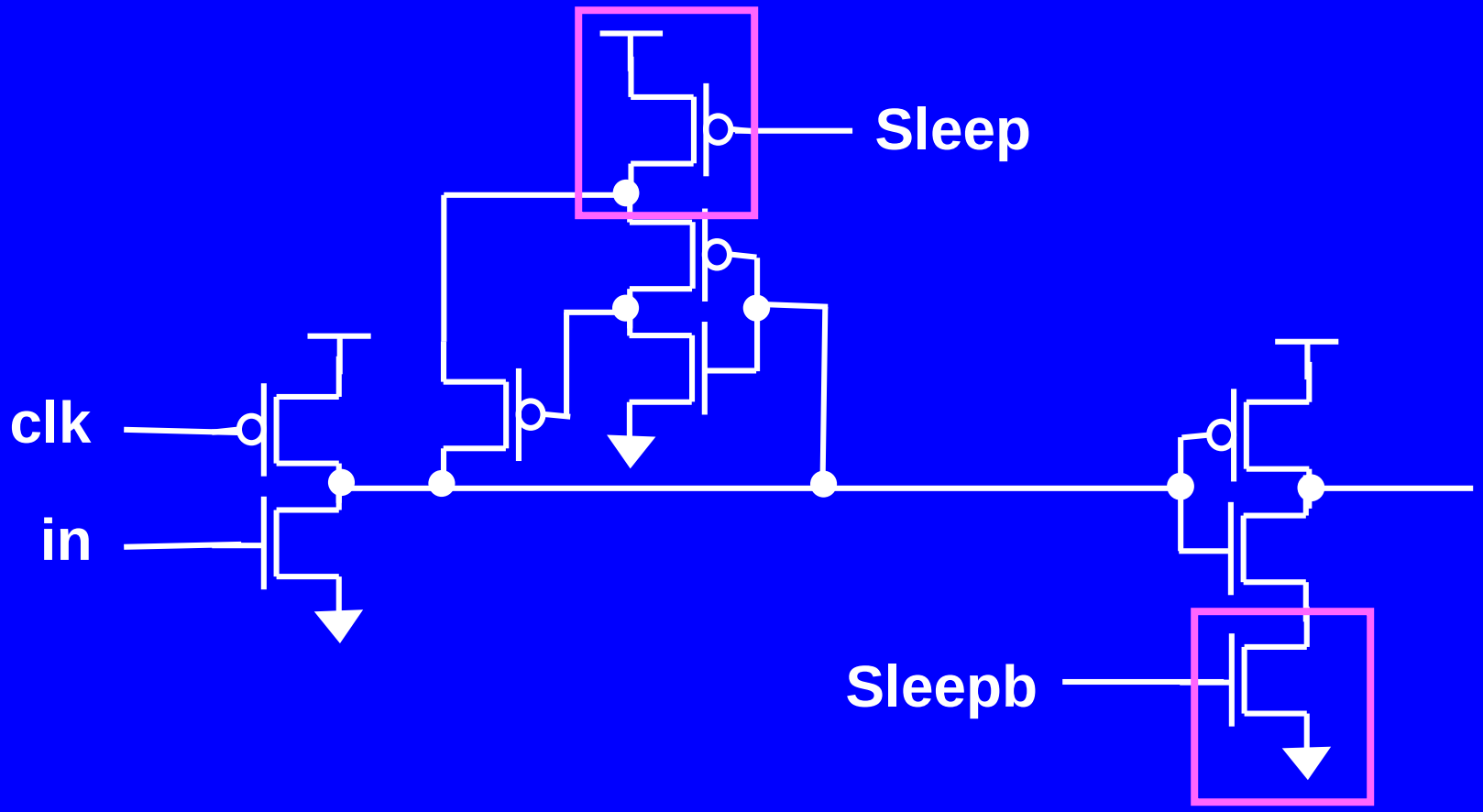


Conventional Domino



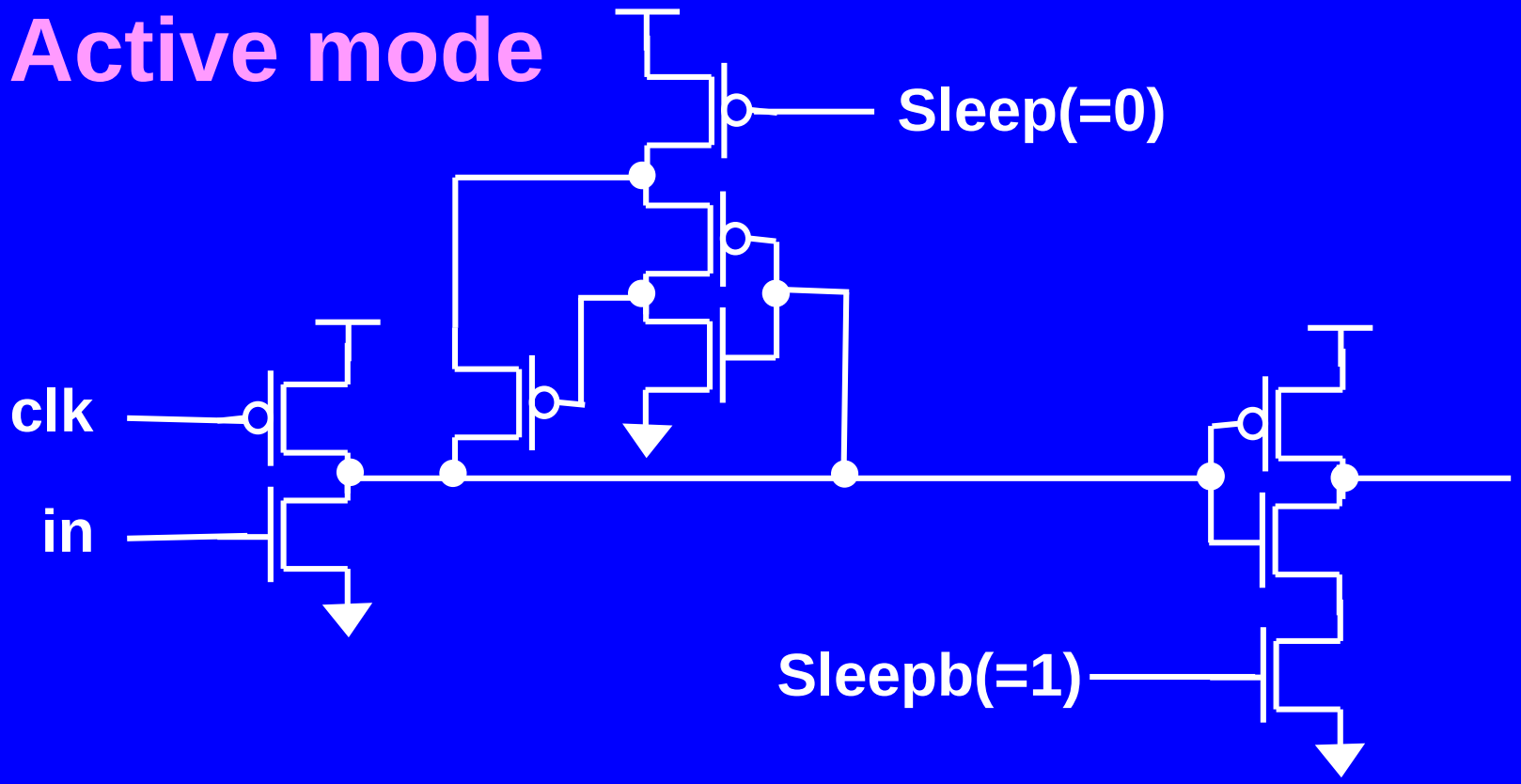
Leakage-Biased (LB) Domino

Two sleep transistors in non-critical path



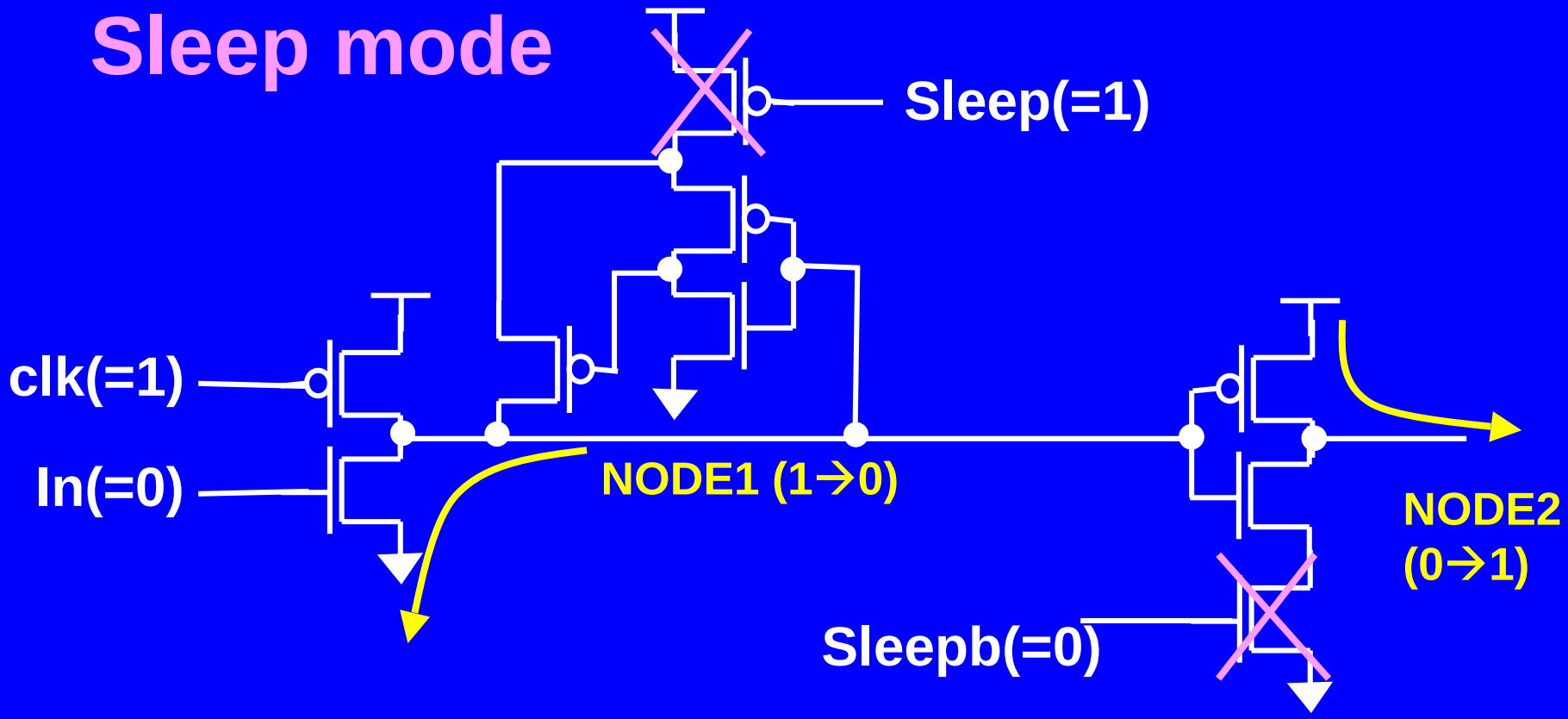
Leakage-Biased (LB) Domino

Active mode



Leakage-Biased (LB) Domino

Sleep mode

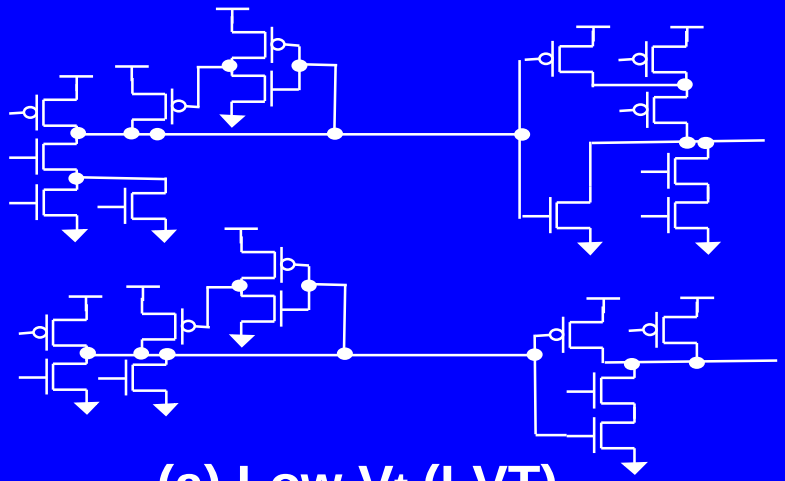


LB-Domino biases itself into a low-leakage stage by its leakage current

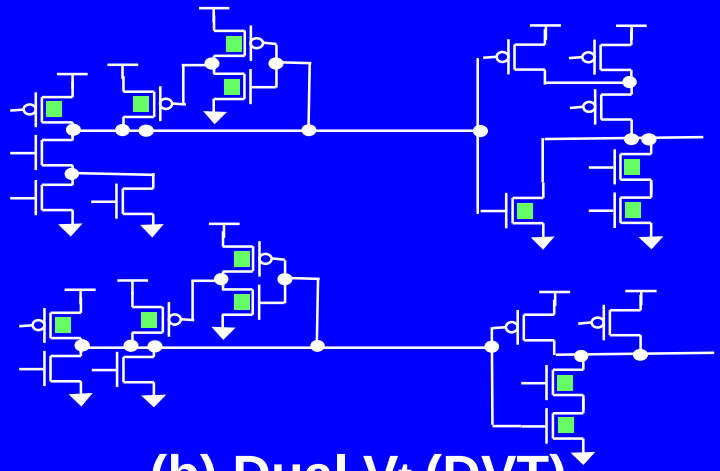
Han-Carlson Adder

- Evaluation with carry generation circuit of a 32-bit Han-Carlson adder
  - 6 levels of alternating dynamic and static logic
  - 4 circuits: LVT, DVT, LB, and LB2
- Constraints
  - Input/Output noise margin kept to 10% of V_{dd}
  - Precharge/Evaluation delay equalized to within 1% error

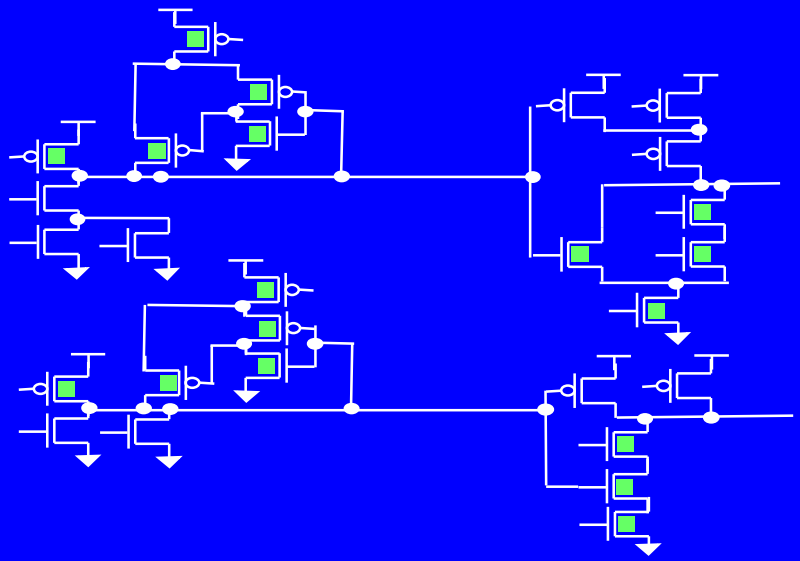
PG Cells of Han-Carlson Adder



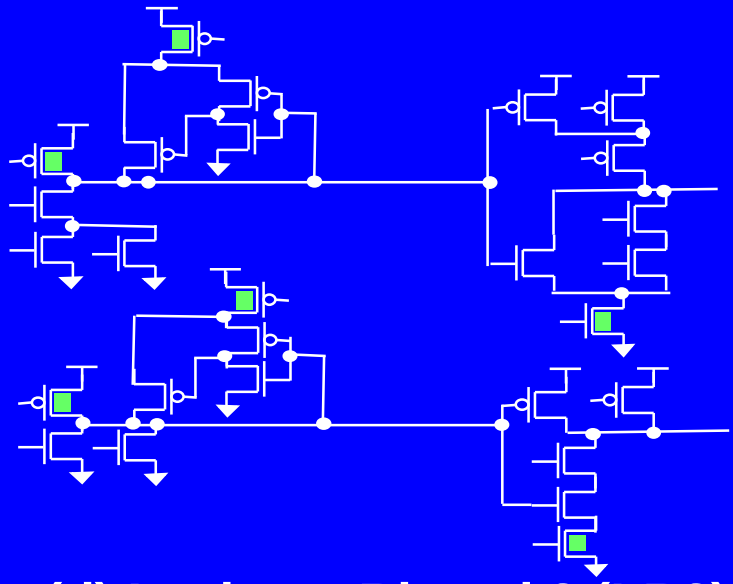
(a) Low Vt (LVT)



(b) Dual Vt (DVT)



(c) Leakage-Biased 1 (LB)



(d) Leakage-Biased 2 (LB2)

Processes

- 180nm: TSMC 180nm Processes
- 70nm: BPTM 70nm Processes

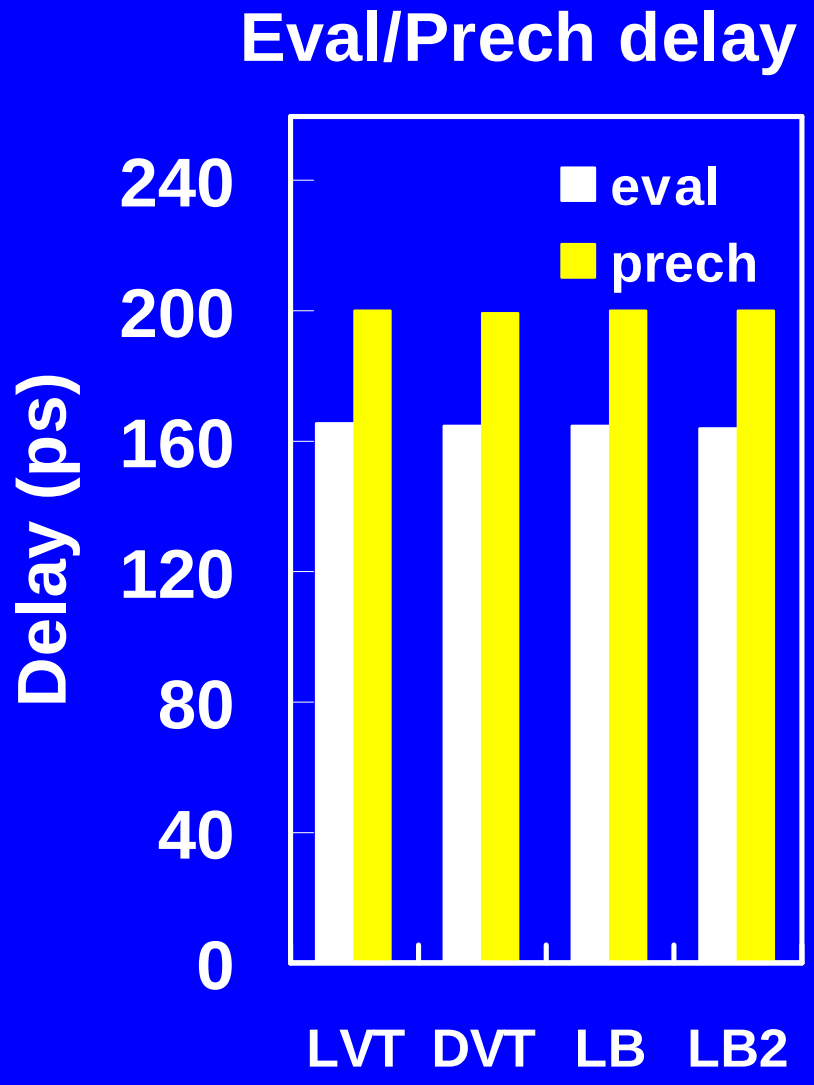
Process	180nm	70nm
High Vt (NMOS/PMOS)	0.46V/-0.45V	0.39V/-0.40V
Low V_t (NMOS/PMOS)	0.27V/-0.23V	0.15V/-0.18V
V_{dd}	1.8V	0.9V
Temperature	100C	100C

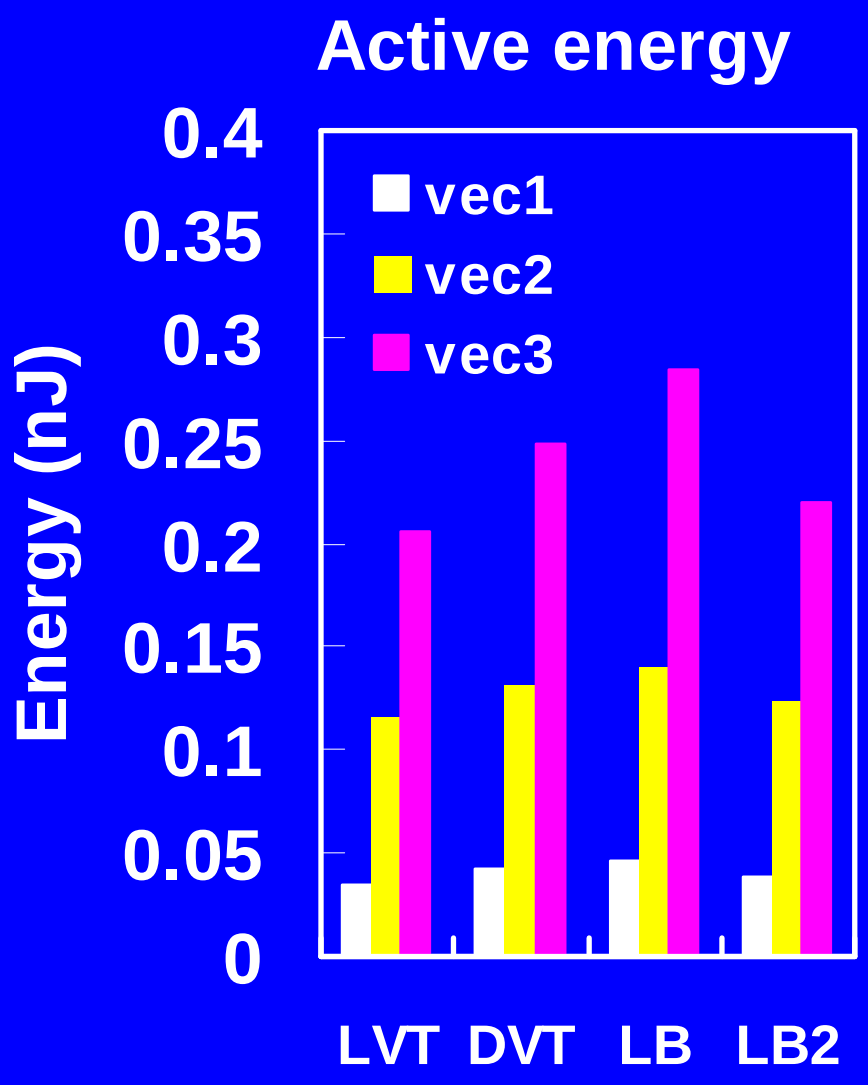
Input Vectors

- 3 different input vectors
  - Active energy and leakage power dependent upon inputs
  - Vec1 discharges no dynamic nodes
  - Vec2 discharge half of dynamic nodes
  - Vec3 discharge all dynamic nodes

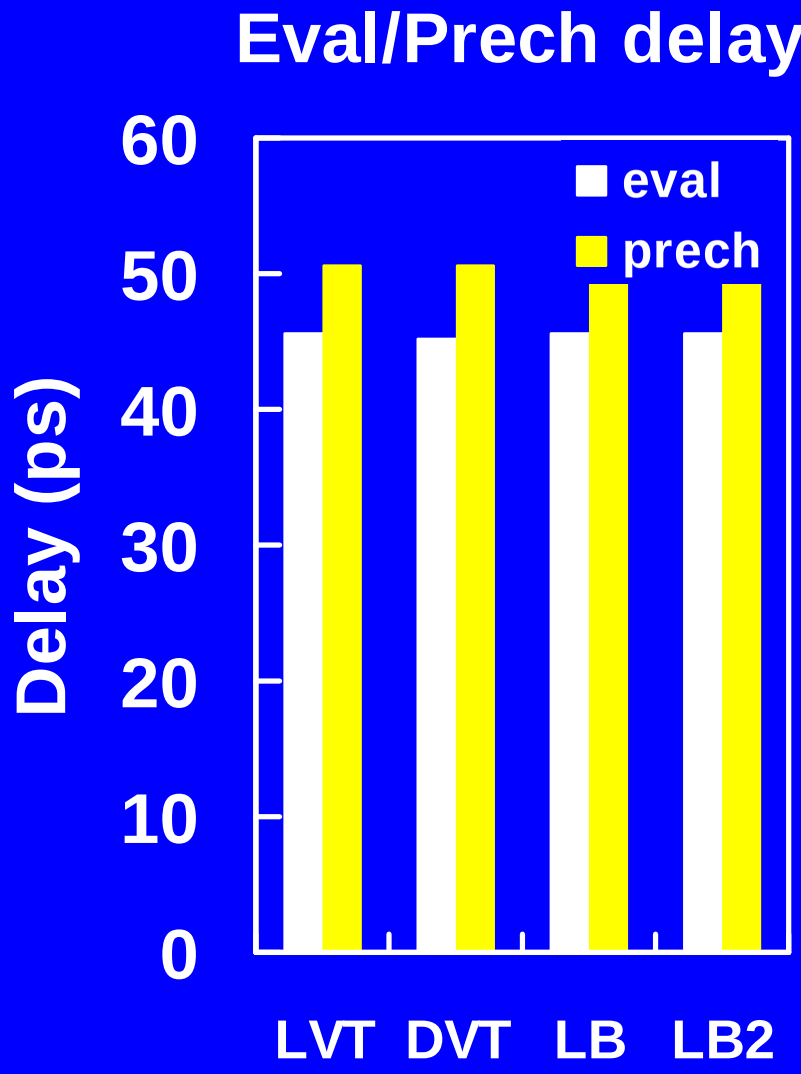
	A	B	Ci
Vector 1	0x00000000	0x00000000	0
Vector 2	0xffffffff	0x00000000	0
Vector 3	0xffffffff	0xffffffff	1

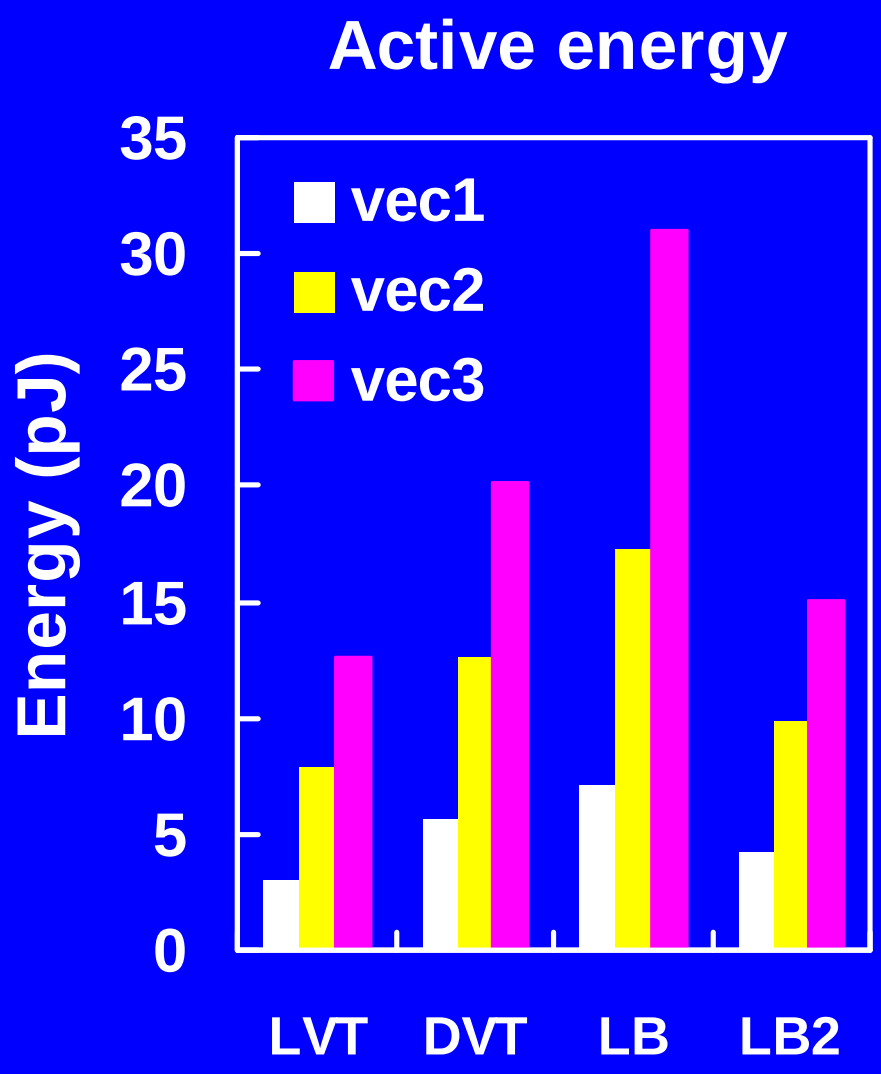
Delay and Active Power: 180nm



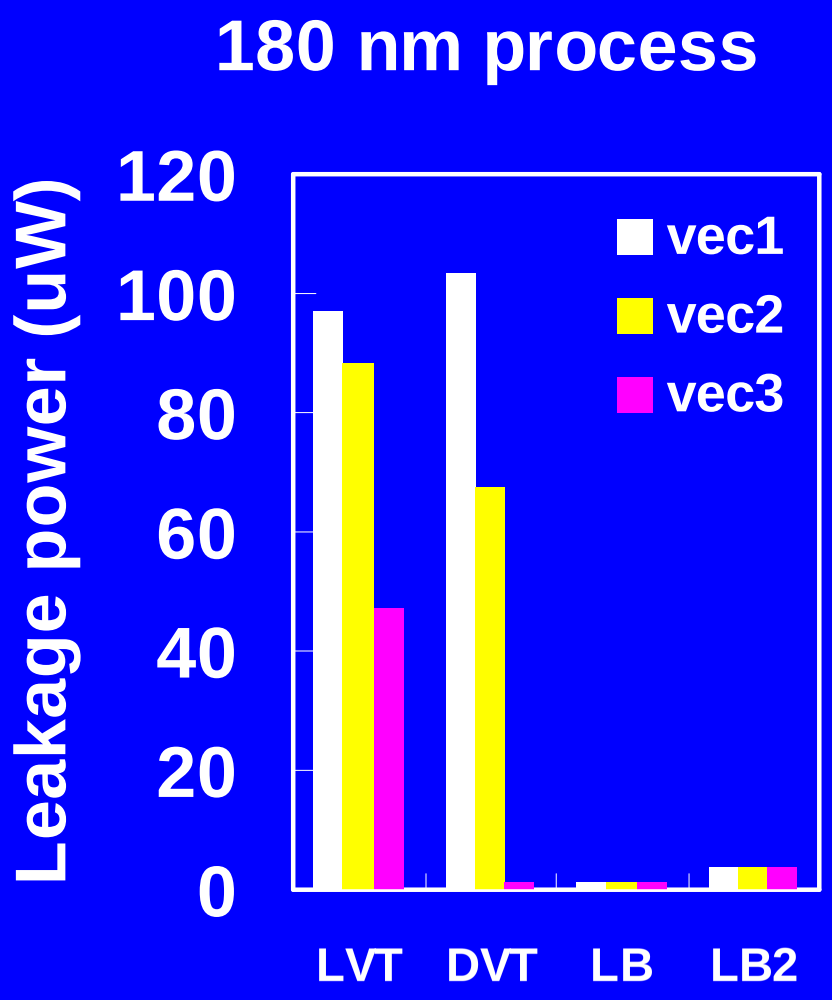


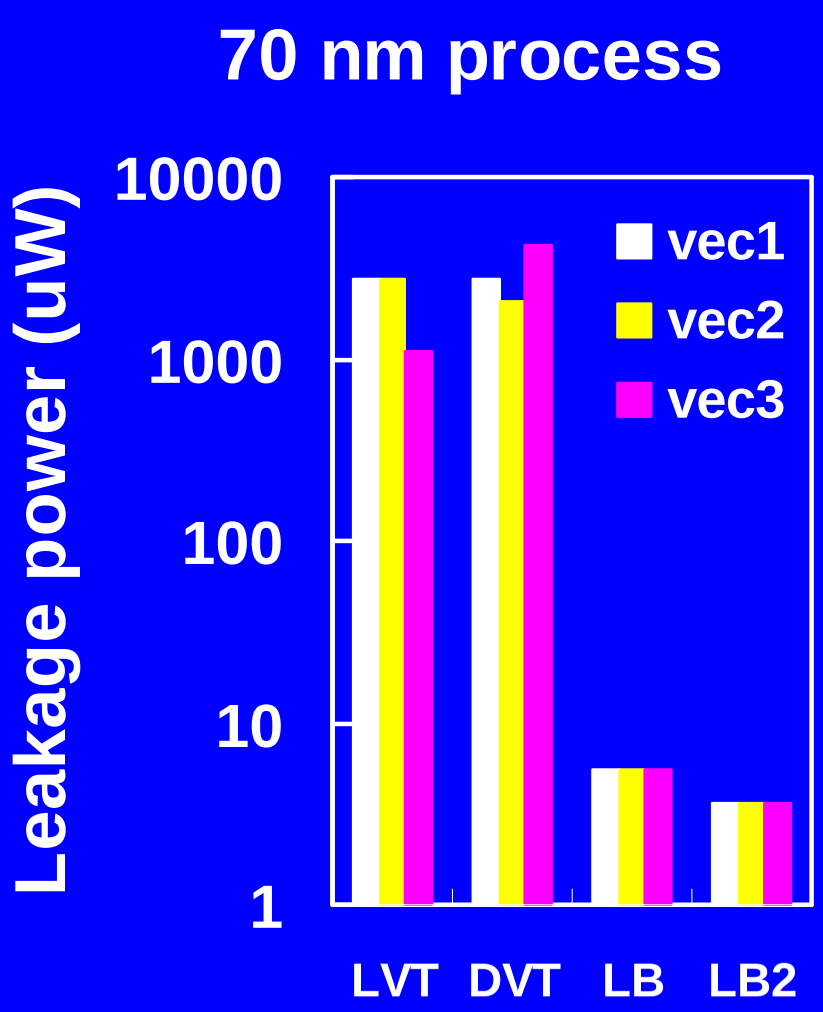
Delay and Active Power: 70nm



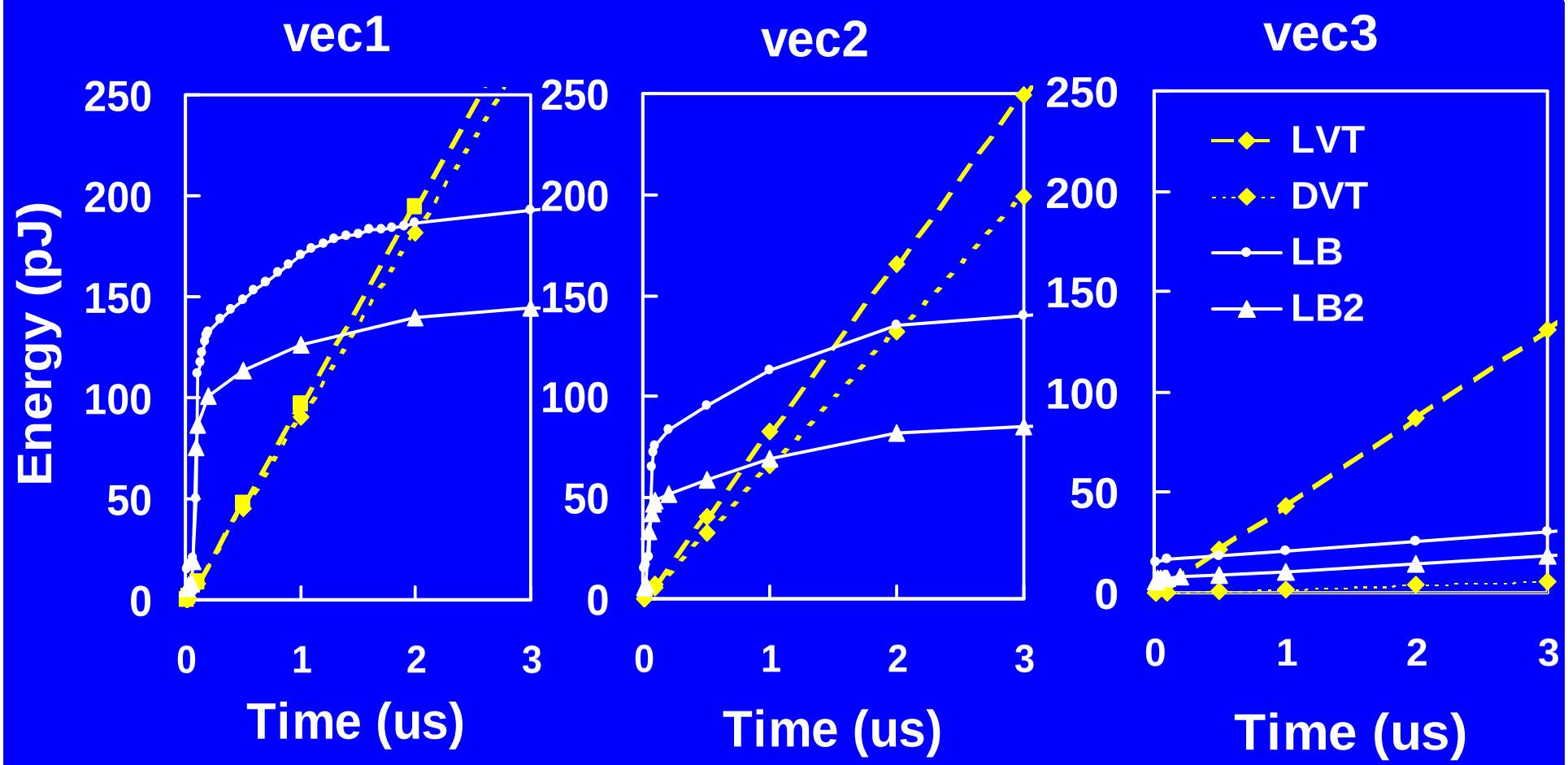


Steady-State Leakage Power

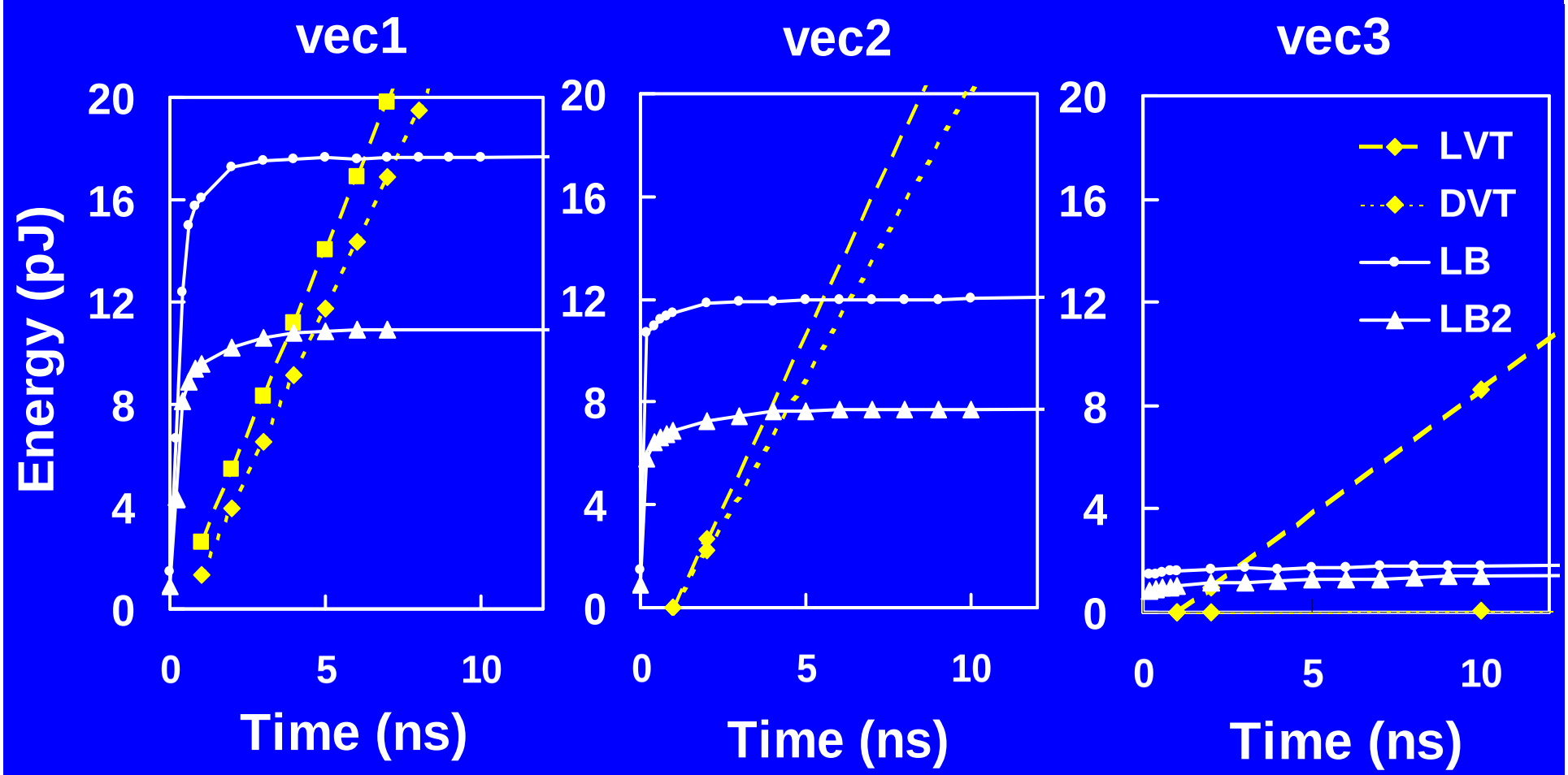




Cumulative Sleep Energy: 180nm



Cumulative Sleep Energy: 70nm



Conclusion

- **Leakage-Biased Idea**
  - ***Leakage can be used to bias nodes into low-leakage states***
- **LB-Domino for Fine-grain leakage reduction**
  - **100x reduction in steady-state leakage**
  - **Low deactivation and wakeup time**
  - **Low transition energy**
    - **>10ns breakeven time at 70nm process**

Acknowledgement

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