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Load-Sensitive Flip-Flop Characterization

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Abstract

Different flip-flop designs vary in the number and complexity of logic stages they contain, and hence have different inherent parasitic delays and output drive strengths. We examine the effect of electrical load on flip-flop delay and energy consumption and show that the relative ranking of optimized flip-flop structures varies widely with both electrical effort and absolute load. We also show that some structures benefit substantially from the addition of appropriate output buffering.

1. Introduction

Timing elements (TEs), including various forms of flip-flop and latch, are one of the most important components in synchronous VLSI designs. Their performance has a critical effect on cycle time and they often account for a large fraction of total system power. Therefore, there has been significant interest in the development of fast and low-power TE circuits, and correspondingly in techniques to evaluate their performance. Previous work in TE characterization [11, 9, 4, 12, 7, 6, 10, 5, 14] has failed to consider the effect of circuit loading on the relative ranking of TE structures. These earlier work used fixed, and usually overly large, output loads when comparing alternatives. Input drive was either assumed to be large [11, 9] or was not specified [12, 7, 6, 10, 8, 15, 5, 14].

In this paper, we show that load effects must be considered in TE characterization to avoid sub-optimal TE selection. TE structures vary greatly in the number and complexity of logic stages they contain leading to a wide variation in parasitic delays, output driving capability, and energy consumption. We present energy and delay curves for a variety of TE structures across a range of output loading conditions and show that relative ranking of structures varies depending not only on the electrical effort (output capacitance divided by input capacitance [13]), but also on the absolute value of the load. We also show that several structures benefit from the addition of appropriate output buffering when driving the larger loads used in earlier studies, and hence have better relative performance than previously reported.

The paper is organized as follows. Section 2 describes our methodology for measuring energy and delay of a given flip-flop structure. Section 3 presents a range of flip-flop structures. Section 4 shows detailed energy and delay analysis of the chosen flip-flop structures. Section 5 concludes the paper.

2. Simulation Test Bench

We implemented our designs using a TSMC 0.25 μm CMOS process. The simulation test-bench we used is shown in Figure 1. To control flip-flop input loading, we use a fixed-size inverter to drive the data input rather than fix an input capacitance for the flip-flop, because this gives more freedom in optimizing the flip-flop energy-delay characteristic. We use a further FO4-loaded inverter to shape the signal fed to the input driver.

The clock buffers were sized for each flip-flop to give equal rise and fall times across all designs. We assumed that both true and complement clocks are made available in buffered form, to avoid unfairly penalizing designs that require complementary clocks.

We use the output energy of the shaded inverters (data and clock) to measure the signal input energy to the flip-flop. We also measure the internal energy the flip-flop draws from the supply, but do not include the output energy dissipated in the load as this is assumed to be due to the next stage's input load.

We measured flip-flop delay using the minimum D-Q delay metric proposed by Stojanović and Oklobdžija [11]. C-Q delay depends on D arrival time, and hence there is an optimal D arrival time which minimizes D-Q delay.

Transistor widths were optimized using Hspice's Levenberg-Marquardt optimization method. Transistor lengths were fixed at minimum, and parasitic information

was included in the circuit netlists used for optimization and simulation. All tests were run under nominal conditions of $V_{dd} = 2.5\,\text{V}$ and $T = 25\,^{o}\text{C}$.

3. Flip-Flop Designs

Figure 2 shows schematics for the flip-flop designs we used in our evaluation. We restricted our evaluation to fully static designs in this paper, but expect similar results on load sensitivity for dynamic registers also. We restricted this study to single-ended signals in and out of the flip-flop, and only loaded one output if the flip-flop structure had complementary outputs. We assumed both true and complement clock signals are available and did not include local clock inverters except where used to generate clock pulses.

Figure 2(a) is a master-slave PowerPC-style flip-flop (PPCFF), which is based on a transmission-gate latch [11]. Figure 2(b) is the StrongARM flip-flop (SAFF) [2]. The output latch is built with coupled NAND gates which limit output drive. Figure 2(c) is a StrongARM flip-flop with a modified output stage (MSAFF) which is claimed to have a faster output stage than SAFF [9]. Figure 2(d) is the hybrid latch flip-flop (HLFF) which is generally known as one of the fastest flip-flops [1]. Figure 2(e) is a pulse latch based on a static sense amp latch (SSAPL) with its own clock pulse generator [4].

4. Energy and Delay Analysis

Figure 3 shows a histogram of output loads for flip-flop instances in a custom-designed MIPS RISC CPU datapath in a $0.25\,\mu$m process [3]. These loads were obtained from two-dimensional extractions including wire and transistor parasitics. From this figure, we see that there is a range of loadings, but many loads are light and that nearly all loads are below 60 fF. For reference, a single minimum-sized inverter represents a load of around 1.8 fF.

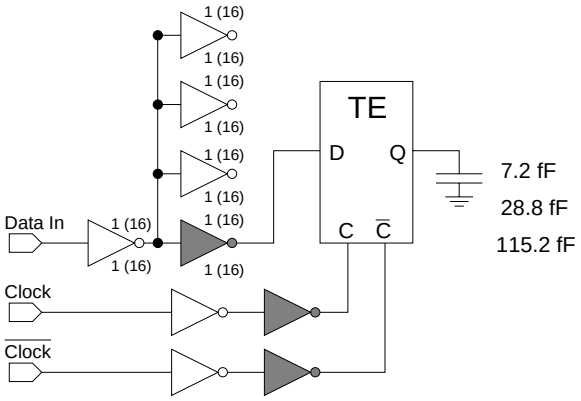

Figure 1. Flip-flop test bench.

4.1. Delay

We measured the minimum delays of the flip-flops for a minimum-sized input driver and three different electrical efforts (EE) : EE4-min (7.2 fF output load), EE16-min (28.8 fF), and EE64-min (115.2 fF), where we measure electrical effort from the input of the input drive inverter directly ahead of the flip-flop. Each flip-flop was resized for minimum D-Q delay at each load point. To show the effects of absolute load on performance, we also measured the minimum delays of the flip-flops for an input driver 16 times larger than minimum driving a load of 115.2 fF, corresponding to an electrical effort of 4 (EE4-big).

Figure 4 presents the results for minimum delay and overall ranking at each load point. We notice that the speed rankings or relative speeds vary according to load size. Performance of PPCFF and SSAPL get relatively worse, but MSAFF and HLFF get relatively faster, as load size increases. Also, we see that the variance between delays gets larger as load size increases. The variance between the slowest and the fastest at EE4-min is less than 0.3 ns, but that at EE64-min is larger than 3.5 ns.

The delay of a flip-flop circuit has two components, the intrinsic parasitic delay of the flip-flop structure and an output drive delay which is proportional to both driving capability and load size. For small loads such as EE4-min, the parasitic delay of a flip-flop structure is usually dominant, but for large loads such as EE64-min, the driving delay is more important than the parasitic delay. Different flip-flop structures have different driving capabilities and different intrinsic delays causing the change in relative performance and the larger variance at higher loads.

The parasitic delays for each flip-flop include parasitics along the signal path, which tend to scale when transistors are sized for larger loads, and parasitics due to state-maintaining feedback paths which do not generally scale with larger load. We can see this effect in Figure 4 where the EE4-big delays are smaller than the EE4-min delays.

PPCFF is the fastest structure at EE4-min, but its delay grows quickly and it ranks third at EE64-min. In fact, PPCFF delay more than triples from EE4-min to EE64-min even though transistors were optimally resized for the larger load. SSAPL is a poorer driver than PPCFF. SSAPL delay is 0.38 ns at EE4-min, but increases to 4.22 ns at EE64-min. On the other hand, MSAFF and HLFF have good driving capabilities. MSAFF is the slowest structure at EE4-min, but ranks third at EE64-min, with only 66% delay degradation. Likewise, HLFF is the fastest structure at EE64-min although it is the second fastest at EE4-min. The delay increases by only 67% from EE4-min to EE64-min.

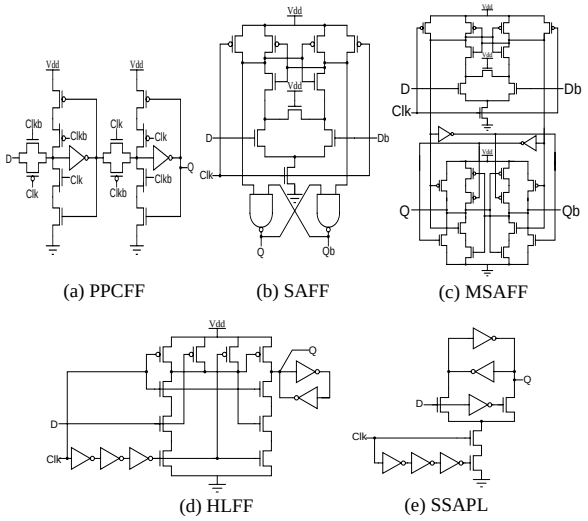

Figure 2. Positive-edge-triggered flip-flop designs.

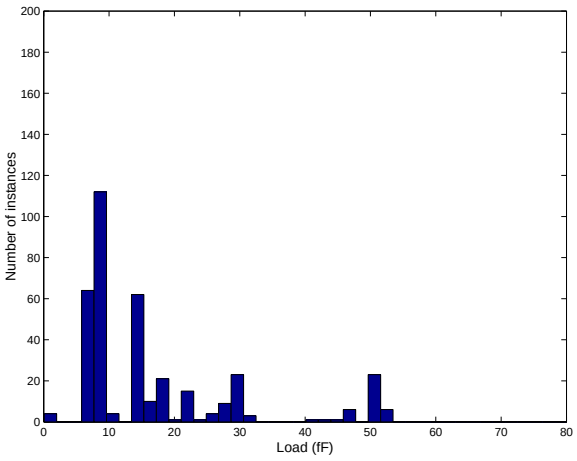

Figure 3. Flip-flop output load instances in a 32-bit microprocessor datapath.

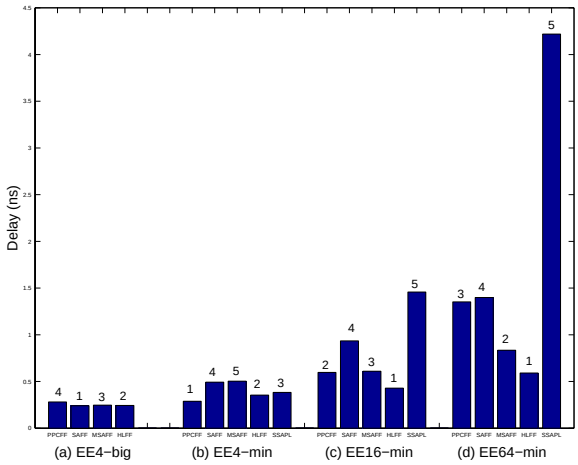

Figure 4. Minimum delay for original flip-flops. Numbers on the top of bars are speed rankings.

In some cases, the performance of flip-flops at higher loads can be improved by simply adding appropriate output buffers and so we studied the use of one or two simple inverters to buffer the outputs. We did not penalize inverting flip-flops because it is not obviously preferable to have true or complement outputs in real system designs.

Figure 5 shows the effects of buffering on the performance of flip-flops. Again, all flip-flops were resized to minimize delay at each load point. Except for HLFF, we see that the slopes of buffered flip-flops are flatter than those of unbuffered ones because the output buffer improves driving capabilities. Also, we see that y-intercepts of buffered ones are higher than those of unbuffered ones, because the additional buffer adds its own parasitic delay. Good drivers like MSAFF and HLFF do not get any speed improvement from buffering, but weak drivers such as SAFF and SSAPL get faster after buffering. SSAPL in particular has large speed improvements, for example, decreasing delay by around 1 ns at EE16-min.

Figure 6 shows the delays of flip-flops after adding buffers when it improves speed. We see that variance between flip-flops become less compared to Figure 4. We note that after buffering, SSAPL becomes a good candidate even at high loads.

These results clearly show that load affects not only absolute performance but also relative performance of different flip-flop structures. It is therefore important to consider loading effects when evaluating different flip-flop designs.

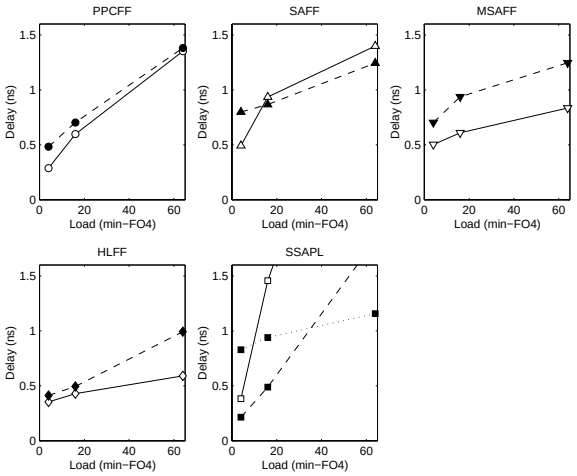

Figure 5. Influence of buffering on minimum delay. Solid line represents unbuffered circuits, dashed line has single inverter buffer, and dotted line has two cascaded inverter buffers. A minimum-sized input driver was used (EE4-min, EE16-min, and EE64-min).

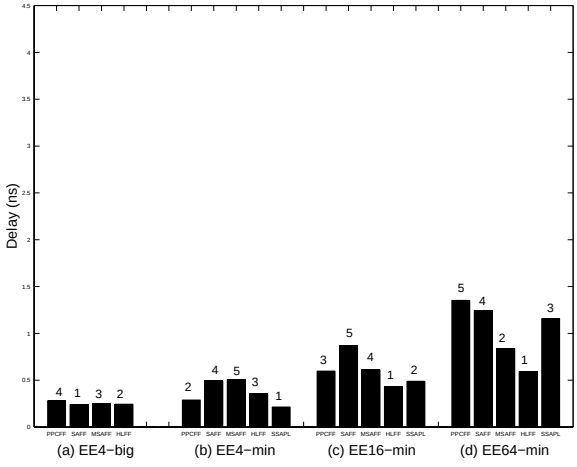

Figure 6. Minimum delay for flip-flops which are allowed output buffering to improve speed. Numbers on top of the bars are speed rankings. SAFF is buffered with one inverter for EE16-min and EE64-min loads. SSAPL is buffered with one inverter for EE4-min and EE16-min loads and with two cascaded inverters for the EE64-min load.

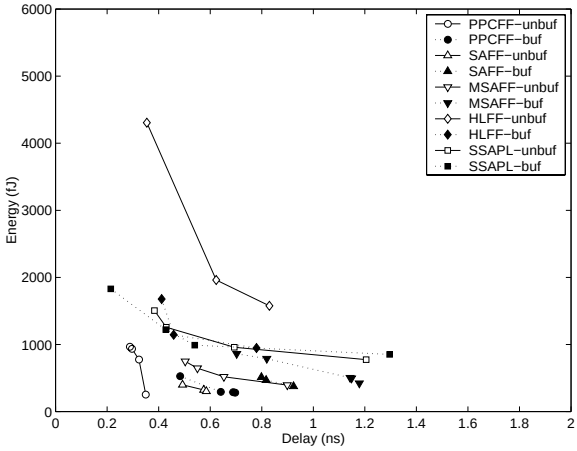

Figure 7. Energy-delay graphs of various flip-flops with a 7.2 fF output capacitance load (EE4-min).

4.2. Energy versus Delay

To determine energy dissipation, we used an input pattern that has an ungated clock and with the input toggling every cycle (just before the positive clock edge for positive-edge-triggered flip-flops). A single pattern is adequate to convey the importance of loading effects on flip-flop energy-delay characterization and allows us to simplify our presentation, but a full characterization of flip-flop energy dissipation should consider more realistic activity patterns [4].

Figure 7, Figure 8, and Figure 9 compare energy-delay graphs of the flip-flops for each load (EE4-min, EE16-min, and EE64-min). Each point on the line was obtained by optimizing a design for minimum energy at the given delay specification.

For EE4-min (Figure 7), PPCFF is the best choice since it shows good performance and also low-energy consumption. Buffered SSAPL has the fastest performance and reasonable power consumption. In this load regime, buffering results in worse energy-delay curves for other flip-flops such as PPCFF, SAFF, and MSAFF. The minimum delay of HLFF is increased after buffering, but its energy consumption is significantly lower.

For EE16-min (Figure 8), we find that unbuffered SSAPL is a poor choice in terms of both energy and delay, while buffered SSAPL is very competitive giving high speed at reasonable energy consumption. HLFF is the fastest design overall by a small margin, but requires a huge increase in energy (off scale in the figure). Buffering lowers HLFF energy significantly by reducing short-circuit currents (buffered HLFF is $1/7$ energy of unbuffered HLFF at 0.5 ns delay) but also increases its minimum delay so

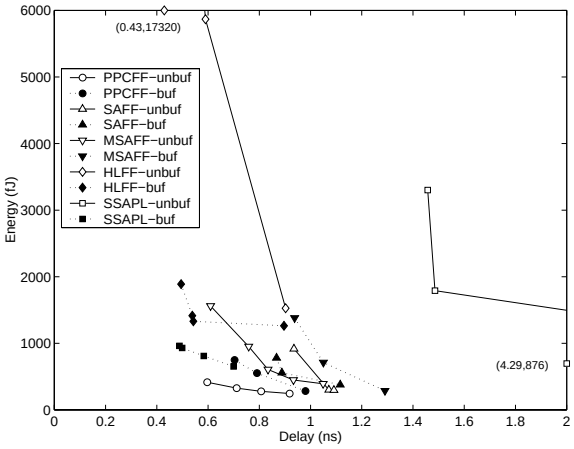

Figure 8. Energy-delay graphs of various flip-flops with a 28.8 fF output capacitance load (EE16-min).

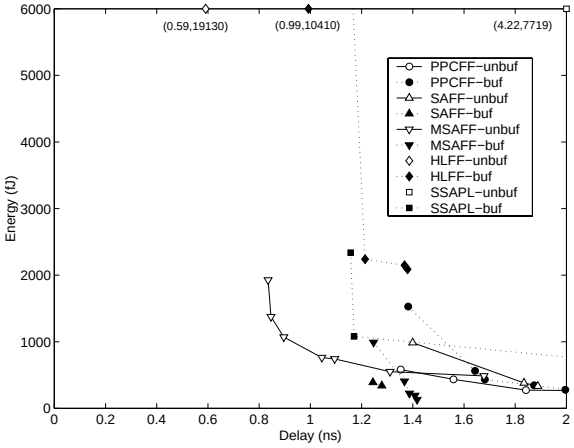

Figure 9. Energy-delay graphs of various flip-flops with a 115.2 fF output capacitance load (EE64-min).

that is now slower than buffered SSAPL as well as being higher energy. For our chosen clock and data activity pattern, buffered SSAPL is the best choice if we want high performance at reasonable energy cost. Unbuffered PPCFF is a good choice for non-critical flip-flops, because it is reasonably fast with the lowest energy.

For EE64-min (Figure 9), unbuffered MSAFF is an attractive choice for the given signal activity. It has the second best performance while keeping energy consumption low. Unbuffered and buffered HLFFs have higher speeds but with large energy penalties.

Figure 10 shows the results for the EE4-big case. This energy-delay graph resembles that of the EE4-min case more than any other case because it tests the same electrical effort. The delay ranges are similar to the EE4-min case, and as with the EE4-min case, buffering is usually not helpful. Also, for both cases, PPCFF is fast and the most energy-efficient, and while MSAFF and SAFF have similar minimum delays, SAFF is more energy-efficient. However, for the EE4-big case, SAFF and MSAFF are faster than PPCFF and HLFF unlike the EE4-min case. This demonstrates that the ranking of flip-flop structures depends not only on the electrical effort, but also on the absolute value of the load and the input drive. The EE4-big case has a smaller feedback penalty than the EE4-min case because the feedback transistors don't scale with the load. Therefore, SAFF and MSAFF, which have many feedback transistors, can excel for the EE4-big case.

These results clearly show the importance of load size and output buffering when comparing flip-flops for energy and delay. For example, at high loads MSAFF is clearly superior to SAFF, as stated in [9], but at low loads the basic StrongARM SAFF design is better than the modified MSAFF design, giving similar speeds with lower energy.

5. Summary

Even though real VLSI designs exhibit a variety of flip-flop output loads, earlier work has evaluated and compared flip-flop designs with fixed, and often excessive, load size. In this paper, we showed that the output load size can greatly affect the relative energy and delay performance of different flip-flop designs, and must be accounted for when comparing flip-flop designs. For example, MSAFF is the second fastest flip-flop in the EE64-min case since it has good output driving capability. On the other hand, MSAFF is the slowest in the EE4-min case due to its relatively large parasitic delay. As another example, MSAFF gives better energy and delay performance than SAFF for large output load. When output load is small, however, SAFF becomes a better choice since it gives similar delay with lower energy consumption.

We also demonstrated that simple output buffering can

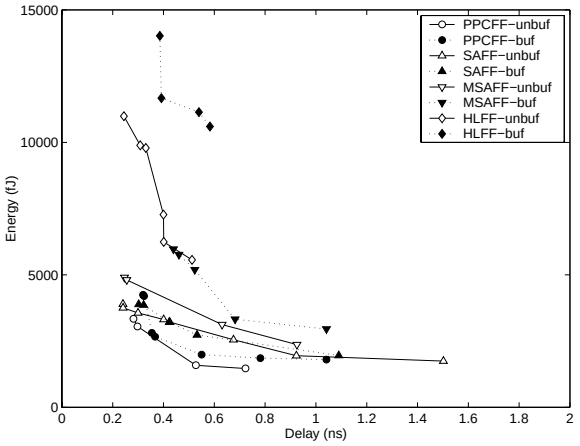

Figure 10. Energy-delay graphs of various flip-flops with a 115.2 fF output capacitance load (EE4-big).

be beneficial to both energy consumption and delay for flip-flop designs even at relatively small loads, thus also needs to be included in comparative studies. For example, SS-APL, which has weak output driving capability, could improve its delay by around 1ns in the EE16-min case simply by adding one output buffer. Also, for the EE16-min case, output buffering could lower HLFF energy by a factor of 7 at 0.5ns delay by reducing short-circuit currents.

References

[1] H. P. *et al.* Flow-through latch and edge-triggered flip-flop hybrid elements. *Digest ISSCC*, pages 138–139, February 1996.

[2] J. M. *et al.* A 160-MHz, 32-b, 0.5-W CMOS RISC microprocessor. *IEEE Journal Solid-State Circuits*, 31(11):1703–1714, November 1996.

[3] S. Heo. A low-power 32 bit datapath design. Master's thesis, Massachusetts Institute of Technology, August 2000.

[4] S. Heo, R. Krashinsky, and K. Asanović. Activity-sensitive flip-flop and latch selection for reduced energy. In *19th Conference on Advanced Research in VLSI*, Salt Lake City,UT USA, March 2001.

[5] H. Kawaguchi and T. Sakurai. A reduced clock-swing flip-flop (RCSFF) for 63% power reduction. *IEEE Journal Solid-State Circuits*, 33(5):807–811, May 1998.

[6] U. Ko and P. Balsara. High performance, energy-efficient D flip-flop circuits. *IEEE Trans. VLSI Systems*, 8(1):94–98, February 2000.

[7] B. Kong, S. Kim, and Y. Jun. Conditional-capture flip-flop technique for statistical power reduction. *Digest ISSCC*, page 290, February 2000.

[8] T. Lang, E. Musoli, and J. Cortadella. Individual flip-flops with gated clocks for low power datapaths. *IEEE Trans. Circuits and Systems-II: Analog and Digital Signal Processing*, 44(6):507–516, June 1997.

[9] B. Nikolić, V. Oklobdžija, V. Stojanović, W. Jia, J. Chiu, and M. Leung. Improved sense-amplifier-based flip-flop: Design and measurements. *IEEE Journal of Solid-State Circuits*, 35(6):876–884, June 2000.

[10] M. Nogawa and Y. Ohtomo. A data-transition look-ahead DFF circuit for statistical reduction in power consumption. *IEEE Journal Solid-State Circuits*, 33(5):702–706, May 1998.

[11] V. Stojanović and V. Oklobdžija. Comparative analysis of master-slave latches and flip-flops for high-performance and low-power systems. *IEEE Journal Solid-State Circuits*, 34(4):536–548, April 1999.

[12] A. Strollo, E. Napoli, and D. D. Caro. New clock-gating techniques for low-power flip-flops. In *ISLPED*, pages 114–119, Rapallo, Italy, July 2000.

[13] I. Sutherland and R. Sproull. Logical Effort: Designing for speed on the back of an envelope. In *Advanced Research in VLSI*, pages 1–16, Santa Cruz, 1991.

[14] J. Yuan and C. Svensson. New single-clock CMOS latches and flipflops with improved speed and power savings. *IEEE JSSC*, 32(1):62–69, January 1997.

[15] V. Zyuban and P. Kogge. Application of STD to latch-power estimation. *IEEE Trans. VLSI Systems*, 7(1):111–115, March 1999.