# **Assam Hardware Testing**

#### **Overview Presentation**

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## **Lab Configuration**



## Lab Configuration



### Host PC

- Pentium III / 800 MHz
- **300 Watt Power Supply**
- **440 BX Chipset**
- **256-512 MB 100 MHz SDRAM**
- **20G HDD, Dual Boot (Linux/Win2K)**

# ■ Misc

Vendor: PCs for EveryoneAccessories: CDRW, PCMCIA

#### **Host-Baseboard Link**

#### Development card converts PCI to a simpler local bus

- Daughtercard connects local bus to the tester baseboard
  - Provides clock
  - □ Line drivers and terminators
- Custom Linux driver



#### **Tester Baseboard (Back)**



#### **Tester Baseboard (Back)**



#### **Tester Baseboard (Front)**



#### **Tester Baseboard (Front)**



#### **Tester Baseboard Features**

#### **Xilinx XC4028XL**

193 User I/O pins (Max)
18K-50K Gates (Typical)
80MHz external, 150MHz internal

- Sixteen voltage-adjustable and current-monitored power supplies
- Controller for temperature control and measurement
- Configurable status and control bits
- Parallel 32 bit data path
- Adjustable frequency clock
- JTAG serial interface to DUTs

#### **Adjustable Power Supplies**

- Voltage adjustable between 0V-3.9V in 1 mV increments
- Current measurements stored in 24 MB DRAM
- Adjustable sample rate
  - □ DRAM can hold 2 seconds at 500 kSamples/s
  - **DRAM** can hold 64 seconds at 15 kSamples/s



#### **Adjustable Power Supplies**





## **Temperature Monitor/Control**



# Bond to chip in a reusable fashion

#### Documentation Issues

- □ Part numbers
- □ Interface to ATC0 PCB

#### Control

- **32** control bits configurable on the baseboard
- Parallel bidirectional datapath between baseboard and DUT (32 bits plus control).

#### Clock

- Clock generator frequency can be specified in 1 MHz steps from 25-400 MHz, using an external crystal as a reference.
- Differential PECL outputs. Must be converted on test chip PCB to a single-ended signal with the appropriate signal levels.

#### **ATC0 Interfaces**

