ATB0 Engineering Document - Hardware

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1 Introduction

This document is one in a set of three engineering documents describing the Assam Tester Basboard 0 (ATB0); this document describes the hardware while the other two describe the controller [1] and the software interface [2].

ATB0 is designed to provide a testbed for custom designed circuit boards that require multiple differing power supplies (referred to in these documents as the "daughtercard"). ATB0 also provides a communication channel between a host PC and the daughtercard. This document gives some design notes concerning the hardware to give a user of ATB0 a general understanding of how each component works, as well as any "gotchas" or tweaks that were done to get things working that may not be included in other documentation.

Figure 1 shows a block diagram of the entire system, showing how data flows from the host PC to the daughtercard. The host PC sends data over the PCI bus to a card made by PLX that forwards data from the PCI bus to various external busses, called herein the "PLX interface card". The PLX interface card sends data for its "local bus 0" to a custom daughtercard connected to the prototyping area on the PLX interface card, this daughtercard is called herein the "PLX daughtercard". The PLX daughtercard sends the data over the long ribbon cable to the Xilinx FPGA on ATB0. The FPGA is configured with the ATB0 controller [1] which controls the power supplies that power the daughtercard and the frequency synthesizer which provides a clock to the daughtercard. It can also forward data directly to the daughtercard via 60 I/O pins connecting ATB0 to the daughtercard. ATB0 also contains SDRAM chips that can hold current measurements from the power supplies until the host reads them back. This allows the current to be measured at a higher sampling rate than would be allowed if each measurement had to be sent back to the host after each sample. ATB0 itself is powered by an external power source.

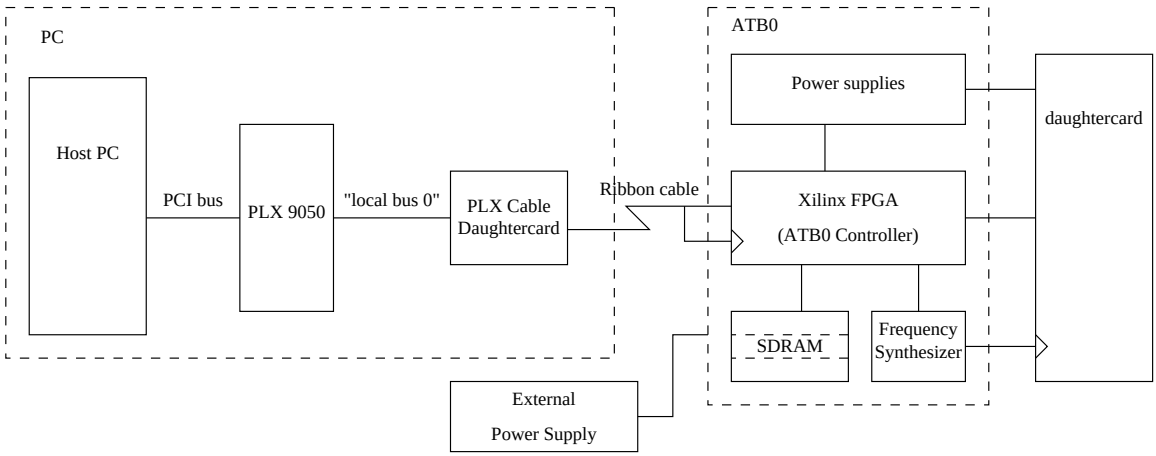

Figure 1: Block diagram of entire system.

This document splits the design into three main pieces. First, getting data from the Host PC to ATB0. This involves the PLX interface card, the PLX daughtercard, and the circuitry on the baseboard to receive the signals, and is described in Section 2. Second, the power supplies are described in Section 3. Finally, the frequency synthesizer and SDRAM modules are described in Section 4.

The best way to gain a thorough understanding of how the baseboard works is to study the schematics and read the datasheets, Section 5 provides some resources to do so.

2 PLX Interface board

The PLX card is a "Rapid Development Kit" (RDK) made by Twin Industries and serves mainly as a host for the PLX 9050 PCI Accelerator chip from PLX and throughout these documents is referred to as "the PLX interface card" or simply, "the PLX". The details of how both the RDK and PLX work is not important to the operation of ATB0, the RDK manual [3] and PLX 9050 databook [4] provide schematics and ample information for the curious reader.

The PLX translates between the PCI bus protocol and legacy protocols such as ISA. It uses a number of "local address spaces" to provide interfaces to more than one device that uses a legacy protocol. Each local address space is assigned a range of physical PCI addresses. When the host PC writes to a PCI address in a local address space's range, the PLX translates it to its own protocol and sends it to the legacy device. We use local address space 0 to communicate with ATB0. To cause the PLX to send local address space 0 to the prototyping area, all jumpers from J14 on the RDK board are removed (otherwise it would go to the on board SRAM). A custom daughtercard, referred to as the "PLX daughtercard" is connected to the prototyping area and forwards memory accesses from the prototyping area to ATB0. The jumpers from J10 are removed as well, as the clock is provided through the PLX daughtercard, so the clock from the RDK is not needed. J13 is all open, and the other jumper blocks have their default loading as described in the RDK manual [3]. In addition to sending local address space 0 to the daughtercard, there are a few signals that are not sent to the daughtercard that need to be wired to it manually, they have something to do with the read/write signals.

Unfortunately the 9050 RDK is no longer sold; it has been replaced by the 9052 RDK. The 9052 chip is supposedly compatible with the 9050, but the development board does not contain the socket into which the PLX daughtercard is plugged. A solution to using the 9052 has been investigated and it might be possible to create a "translator" to use the 9052 if it becomes necessary.

Once the data signals, which comprise of a 32 bit bus, about 10 control signals, and a couple of User I/O pins, get to the PLX daughtercard, fast CMOS 16-bit bidirectional transceivers [5] are used to send the signals over the long ribbon cable. The PLX daughtercard also provides the clock for most of the system using a crystal oscillator that is fed into a programmable skew clock buffer [6] then to the transceivers and over the ribbon cable. Two copies of this clock, one that is slightly delayed, are sent across the cable; currently only one of them is used.

On ATB0, on the other side of the ribbon cable, matching transceivers receive the signals and feed them directly into the Xilinx FPGA. One of the signals on the ribbon cable is the clock created on the PLX, this clock is used by the Xilinx as the global clock for the entire system. The Xilinx on the FPGA is a Xilinx XC4028xl [7] with a speed grade of -1 and in the hq240 package. The configuration pins of the Xilinx are tied to specific inputs from the PLX to allow it to be programmed via the PLX. The the mode pins are tied select the Peripheral Asynchronous configuration mode (101). The PRGM input is tied to HRESET_B so a reset of the local bus begins configuration of the Xilinx, the WS input is tied to HWRITE_B which is the write strobe that indicates data is being sent, and the 8 configuration data (CFD) pins are tied to the bottom 8 pins of the main 32 bit bus. The DONE output is tied to the signal that becomes the USER0 pin on the PLX and the RDY signal is tied to what becomes the USER1 pin on the PLX. The active low INIT input is tied high but connected to ground through a button on the baseboard to allow the user to manually reset the FPGA. The INIT signal can also be probed at the software level, which can be useful for debugging purposes. See the schematics [8] for diagram of all connections between the PLX and the Xilinx.

In addition, the JTAG configuration pins are sent to a jumper on the baseboard so the Xilinx can be configured directly with JTAG. The reset signal to the DACs that set the voltage of the power supplies

Power Supplies	Maximum Current	Voltage Range
0 - 3	4000 mA	0 - 4*V*
4 - 7	800 mA	0 - 4*V*
8 - 13	150 mA	0 - 4*V*
14 - 15	100 mA	0 - $-4V$

Table 1: Current and voltage ratings for the power supplies.

(PVSRSB) has a connection to ground through an additional button so the power supplies can be quickly reset to zero. Other than these special connections, all the pins on the Xilinx are either used as I/O from the PLX, components on the baseboard, or the daughtercard.

3 Power supplies

ATB0 contains sixteen independent power supplies that can be configured to supply a voltage independently of each other; there are fourteen power supplies that supply a positive voltage between 0 and 4 volts and two that supply a negative voltage between 0 and -4 Volts. The power supplies also differ in the amount of current they can supply. The ratings for each of the power supplies is summarized in Table 1. The power supplies have three main operations: setting the voltage, measuring the current, and measuring the voltage. A schematic of an entire power supply is shown in Figure 2. Other than moving a few components around and adding some names, this is the same as the power supplies in the full schematics [8].

3.1 Setting the voltage

The power supplies use a combination of a digital to analog converter and a voltage regulator to set the voltage. The DAC is used to generate the desired voltage then the voltage regulator is used to drop the supply voltage down to the desired voltage. The DACs used are are Maxim +5V, Low-Power, Voltage-Output, Serial 12-Bit DACs (MAX531) [9] and are daisy chained together with the data out (DOUT) of one DAC the data in (DIN) of another (except for the first DAC, whose DIN is PVSDI9 from the controller). This works because "the data at DIN appears at DOUT, delayed by 16 clock cycles plus one clock width" [9]. Therefore, a single serial data line, PVSD, can be used to set the voltage output (VOUT) of all the 16 DACs. The chip select (CS) comes from the controller on the Xilinx (PVSCSB) as does the reset signal (CLR/PVSRSB) and the clock (SCLK/PVSCLK). RFB is tied to VOUT and REFI, REFO, and BPO are all tied to ground, causing the DAC to use its internal reference voltage of 2.048 V in a unipolar configuration with gain of +2. This causes the DAC to have an output range of 0 V to 4.095 V. A small capacitor is placed between the reference pins and ground to reduce noise. This is the setup shown in Figure 7 of the datasheet [9]. See the controller documentation [1] for an explanation of how to determine the value to write to the DAC to produce a given voltage.

Once the DAC has set VOUT to the desired voltage it needs to be dropped 1.25 V because the voltage regulator developes a 1.25 V reference voltage between the output and the adjust terminal. This is accomplished using a micropower voltage reference (zener) diode [10]. The output of this zener diode is connected to the adjust (ADJ) input of the voltage regulator. The output is also connected to ground through a capacitor. The VIN of the voltage regulator is the 5 V supply. The end result is the output voltage of the power supply is the same as the voltage on the DAC's VOUT, but is driven by the main power supply, not the DAC. The output of the regulator is connected to ground through a 22 μF capacitor "to ensure good load transient

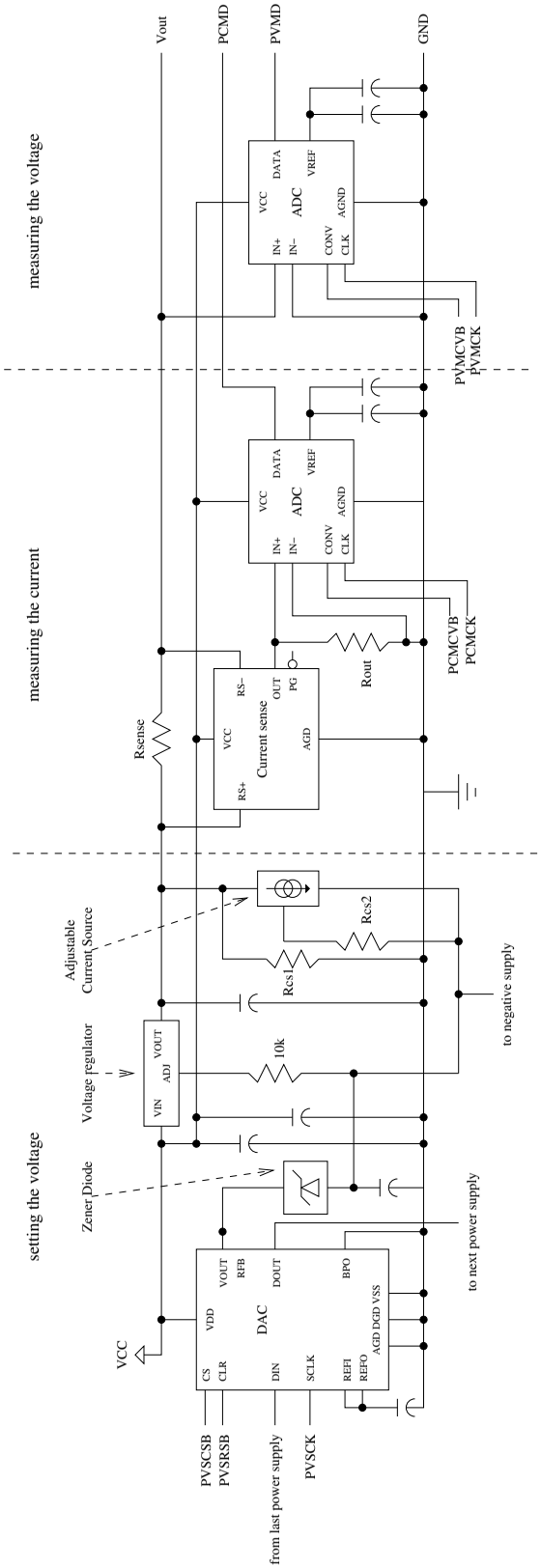

Figure 2: Schematics of a single power supply.

response with large load current changes" [11] (i.e. supply decoupling). Note that because the voltage is actually produced by the voltage regulators, the maximum voltage of the power supply is limited by the dropout voltage of the regulators and may not be the theoretical maximum of 4.095 V (Jim, the designer, expects the maximum to be around 3.9 V).

The voltage regulators are Linear Technology low dropout positive adjustable regulators. Three different sizes are used, one of two different packages of the 800 mAmp LT1117 [11] are used with most power supplies, but the 4.6 Amp LT1585 [12] is used on four of the power supplies to provide a larger current. Because of this, the power supplies differ in the amount of current they are able to provide. Table 1 shows the maximum current of each power supply.

These regulators require a small amount of current, independent of the voltage, to operate correctly. To ensure there is always a current, a current source is used. The current sources are National Semiconductor 3-terminal adjustable current sources (LM334) [13]. The current they provide is determined by the value of R_{cs1} and R_{cs2} and varies depending on the size of the power supply and is the difference between the 800 mA power supplies and the 150 mA supplies. These current sources affect the current mesurements of the power supply; this needs to be taken into consideration when measuring the current.

The two negative power supplies work in similar fashion, except the voltage regulators are replaced with inverting opamps designed to drive 100 mA, and they do not have circuitry to measure the voltage and current. The opamps used are Analog Devices 200 mA output current high-speed amplifiers (AD8010) [14]. The negative voltage to the amplifier is generated using a Power-One DSP-1 series power supply [15]. This negative voltage is also used to drive the current sources in the positive power supplies. A zener diode is used to help regulate this negative voltage.

3.2 Measuring the current

To measure the current, a sense resistor (R_{SENSE}) is placed in series with the output voltage to generate a floating voltage drop. A Maxim high-side current-sense amplifier [16] is used to convert this floating voltage drop across the sense resistor to a ground-referenced voltage. The Power Good (PG) pin of the current sense chip is not used and left floating. The full 5V main power supply is used as the VCC to the current sense chip and the common ground is used. The output of the current sense chip is tied to ground through a resistor, R_{OUT}, as described in the datasheet. Together, R_{SENSE} and R_{OUT} determine the output range of the current sense chip, so these change depending on the range of currents the power supply can supply.

The output voltage from the current sense chip goes into an ADC to be converted into a digital value that can be sent back to the user or written to the SDRAM. A separate serial data line, PCMD#, is used for each power supply to send the data back to the controller on the Xilinx. The ADCs used are Burr-Brown 12-Bit high speed low power sampling analog-to-digital converters (ADS7818) [17]. Again the main 5V power supply is used as the VCC input. The VREF pin is connected to ground through a small 0.1 μF and a large 2.2μF capacitors to keep it stable and cause the ADC to use the internal reference voltage of 2.5 V, causing the output value to range linearly with the input ranges between 0 V and 5 V (twice the reference voltage). The CONV and CLK inputs for every current measure ADC come from the same outputs of the controller, PCMCVB and PCMCK. The positive input to the ADC is the output of the current sense chip. The negative input is tied to ground because the current sensor is a ground referenced voltage.

To calculate the current from the value read by the ADC (x in the equations below), we first need to look at the voltage output of the current sense amp, this is found in the datasheet [17] on page 6 and is repeated in Equation 1. Equation 2 gives the value of the ADC based on its input voltage, which is V_{OUT}, and its reference voltage V_{REF_ADC}, which is 2.5 V. Putting these two equations together gives Equation 3

Power Supplies	Maximum current	R_{SENSE}	R_{OUT}	$\frac{mA}{bit}$
0 - 3	4000 mA	0.033Ω	$2.32k\Omega$	1.5900
4 - 7	800 mA	0.100Ω	$3.83k\Omega$	0.3180
8 - 13	150 mA	1.000Ω	$3.83k\Omega$	0.0318

Table 2: Conversion ratios for calculating current.

and rearranging gives Equation 4 which gives the mA/bit of the value sent from the ADC, which is the conversion ratio to convert from a returned value to the current. Table 2 gives values for each of the three sizes of power supplies. This is in theory. In practice the power supply should be calibrated as described in the controller documentation [1].

$$V_{OUT} = (G_m) * (R_{SENSE} * R_{OUT} * I) \tag{1}$$

$$x = V_{OUT} * \frac{2^{12} - 1}{2 * V_{REF\_ADC}} \tag{2}$$

$$x = (G_m) * (R_{SENSE} * R_{OUT} * I) * \frac{2^{12} - 1}{2 * V_{REF\_ADC}} \tag{3}$$

$$\frac{I}{x} = \frac{1}{G_m * R_{SENSE} * R_{OUT}} * \frac{2 * V_{REF\_ADC}}{2^{12} - 1} \tag{4}$$

$$= \frac{1V}{10mA * R_{SENSE} * R_{OUT}} * \frac{5V}{4095} \tag{5}$$

3.3 Measuring the voltage

A second ADC is used to provide a measurement of the voltage that is actually seen across the power supply. The positive input of the ADC is connected directly to the output voltage, the negative input to ground. A seperate PVMCVB# signal from the controller is used as the CONV input to each ADC, the CLK signal comes from the controller as PVMCK. The reference voltage is setup in the same way as the current measure ADC to use the internal reference so the output value ranges linearly with the input in the range of 0 V to 5 V and the DATA output is sent back to the user via PVMD, a serial data line shared by all of the voltage measure ADCs. See the controller document [1] for a description of how to convert this returned value into a voltage.

4 Frequency synthesizer and SDRAM chips

4.1 Frequency synthesizer

The frequency synthesizer on the baseboard is a Micrel programmable frequency synthesizer (ClockWorks SY89429A) [18] and is used to generate a clock that is sent to the baseboard in the form of a differential PECL output. The XTAL1 and XTAL2 reference frequency inputs are connected to an external 16 MHz crystal to form an oscillator. The Serial Load (SL), Serial Data (SD), and Serial Clock (SC) inputs come from the controller as CKSL, CKSD, and CKSC. The parallel input for M is tied to ground and the parallel

input for N is left floating. The P_LOAD input, which loads the parallel inputs into the chip, is connected to a Dallas Semiconductor 5V EconoReset (DS1233) [19] which is a reset generator, this is meant to load the default frequency of the frequency synthesizer on power up; however, this does not seem to work. Both the positive and negative frequency outputs (FOUT) are sent directly to the daughtercard, the TEST output is sent to a connection on the baseboard for debugging purposes and the loop filters are connected together through parallel capacitors with a resistor inbetween.

The frequency generated is controlled by two configuration values M and N. Basically, the 16 MHz external reference frequency is divided by 8 to be 2 MHz and used as a reference frequency of a phase detector within a PLL. The output of the voltage-controlled oscillator (VCO) within the PLL is forced to be M times this reference frequency. For some values of M (either too high or too low) the PLL will not achieve loop lock, so M must be between 200 and 400. The output of the VCO is further divided by one of four ratios (2, 4, 8, or 16) depending on the value of N (0 divides by 2, 1 divides by 4, etc). The result is an output frequency equal to the external reference frequency divided by eight and multiplied by the ratio of M to N, as shown in Equation 6.

$$FOUT = (\frac{FXTAL}{8}) * \frac{M}{N} \tag{6}$$

An additional configuration value T determines which internal node is sent to the TEST output to be viewed externally. For these values, see the datasheet [18]. Because the parallel interface is not used, and the intended power up sequence does not work, T, N, and M must be configured by the ATB0 controller using the serial interface. See the controller document [1] for a description of the protocol used to do so.

Also note that the datasheet for the frequency synthesizer [18] has a bug (or confusion) in which the "S_LOAD" is used instead of "$\overline{S\_LOAD}$".

4.2 SDRAM chips

The on board SDRAM is three chips that are are Micron SDRAM 4 Meg x 4 x 4 banks (MT48LC16M4A2) [20]. These are connected together to make them appear as a single module that has 2^{26} 12-bit locations. All address and control signals are sent to all three modules. The data is divided into three 4 bit segments and each one is sent to an individial SDRAM chips. All pins on all the chips are connected to the Xilinx so the controller can drive them, except for ground which is tied to the global ground. See the controller document [1] for a description of how the controller interfaces with the SDRAM.

5 Reading the schematics

The schematics [8] for ATB0 are split across six pages with an additional page for the small PLX daughtercard to drive the cable with. The first page of the schematics shows the buffers and transceivers that pull the signals off the cable, the Xilinx FPGA, and the connections to the daughtercard. The second page shows the frequency synthesizer, LGA and LEDs, fixed power supplies, and the SDRAM modules. Pages three through six then contain the 16 power supplies, with a negative power supplies on page three and five. Table 3 tells what each "U" component is to help in reading the schematic. Table 4 is the same thing for the single page schematic for the PLX cable.

A few pin numbers have changed since the schematics were created. There are also a few omissions. Differences between the schematics and the actual pin numbers are listed in Table 5. A complete listing of

Schematic Reference	Compenent name
U1, U2, U3	Pericom Fast CMOS 16-bit Bidirectional Transceivers (PI74FCT16245T)
U4	Xilinx XC4028xl-1-hq240 FPGA
U5	Micrel Programmable Frequency Synthesizer (ClockWorks SY89429A)
U6	Dallas Semiconductor 5V EconoReset (DS1233)
U7, U8, U9	Micron Synchronous DRAM (MT48LC16M4A2)
U10, U11	LEDs
U12, U16, U20, U24, U27, U31, U38, U41, U44, U47, U51, U53, U55, U60, U68, U73, U76, U78, U80, U84, U91, U95, U98, U101, U105, U107, U112, U113	Burr-Brown 12-Bit High Speed Low Power Sampling Analog-To-Digital Converter (ADS7818)
U13, U17, U23, U30, U43, U50, U56, U59, U70, U71, U77, U83, U97, U104, U108, U111	Maxim +5V, Low-Power, Voltage-Output, Serial 12-Bit DACs (MAX531)
U14, U22, U29, U36, U40, U42, U49, U58, U65, U75, U82, U89, U94, U96, U103, U110	National Semiconduct Micropower Voltage Reference Diode (Zener Diode) (LM385-1.2)
U15, U21, U39, U57, U62, U67, U74, U92, U93, U109	Linear Technology 800mA Low Dropout Positive Regulators Adjustable (LT1117)
U18, U66	Analog Devices 200 mA Output Current High-Speed Amplifier (AD8010)
U19, U25, U26, U37, U46, U54, U63, U69, U72, U79, U90, U99, U100, U106	Maxim Low-Cost, Precision, High-Side, Current-Sense Amplifier (MAX4172)
U28, U48, U81, U102	Linear Technology 4.6A Low Dropout Fast Response Positive Regulators Adjustable (LT1585)
U32, U33, U34, U45, U52, U61, U64, U85, U86, U87, U114, U115, U116, U117	National Semiconductor 3-Terminal Adjustable Current Sources (LM334)
U35, U88	Power-One DSP1 Series (DSP1N5S5) (Negative Power Supply)

Table 3: Schematic reference for ATB0

Schematic Reference	Component name
U1, U5, U6, U7, U9	Buffers?
U2	Cypress Programmable Skew Clock Buffer (CY7B991)
U3, U8, U10	Pericom Fast CMOS 16-bit Bidirectional Transceivers (PI74FCT16245T)
U4	Crystal Oscillator

Table 4: Schematic reference for PLX cable

Pin name	Number in schematics	Actual number
SDRAS	134	142
SDD05	142	134
PCMD11	195	205
SDD10	-	148
SDD4	-	141
SDA6	-	159
SDA0	-	152

Table 5: Differences between the schematics and the actual board.

differences between the schematics and the present baseboard can be found in the Assam cvs repository in `atb0/doc/schematics/baseboardR1R2.pdf`.

References

[1] Jared Casper. *ATB0 Engineering Document - Controller*.
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[2] Jared Casper. *ATB0 Engineering Document - Software*.
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[4] *PLX 9050-1 Data Book*.
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[5] *Pericom Fast CMOS 16-bit Bidirectional Transceivers (PI74FCT16245T)*.
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[7] *Xilinx XC4000E and XC4000X Series Field Programmable Gate Arrays*.
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[8] *ATB0 Schematics*.
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[9] *Maxim +5V, Low-Power, Voltage-Output, Serial 12-Bit DACs (MAX531)*.
`assam cvs: atb0/doc/datasheets/MAX531_DAC.pdf`.

[10] *National Semiconductor Micropower Voltage Reference Diode (LM385-1.2)*.
`assam cvs: atb0/doc/datasheets/LM385-ZenerDiode.pdf`.

[11] *Linear Technology 800mA Low Dropout Positive Regulators Adjustable (LT1117)*.
`assam cvs: atb0/doc/datasheets/LT1117_regulator.pdf`.

[12] *Linear Technology 4.6A Low Dropout Fast Response Positive Regulators Adjustable (LT1585)*.
`assam cvs: atb0/doc/datasheets/LT1585_regulator.pdf`.

[13] *National Semiconductor 3-Terminal Adjustable Current Sources (LM334)*.
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[14] *Analog Devices 200 mA Output Current High-Speed Amplifier (AD8010)*.
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[15] *Power-One DSP 1 Series (DSP1N5S5)*.
`assam cvs: atb0/doc/datasheets/DSP1N5S5_negativePowerSupply.pdf`.

[16] *Maxim Low-Cost, Precision, High-Side Current-Sense Amplifier (MAX4172).*
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[18] *Micrel Programmable Frequency Synthesizer (ClockWorks SY89429A).*
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[19] *Dallas Semiconductor 5V EconoReset (DS1233).*
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[20] *Micron Synchronous DRAM (MT48LC16M4A2).*
`assam cvs: atb0/doc/datasheets/64MSDRAM_C.pdf`.