6.893

“A comparison of Full and Partial Predicated Execution Support for ILP Processors”

Serhii Zhak

10/26/2000

Full Predication Support vs. Partial Predication Support

Full Predication Support:

- most flexibility and largest potential performance improvements
- computation of predicate values is highly efficient and parallel

Partial Predication Support

- requires very little change to existing architectures
- increase in the number of instructions executed and requires a larger number og registers to hold intermediate values

ISA Extentions

Extentions for Full Predication Support

Suppression of Execution

Expression of Condition
- predicate register file
- set of predicate instructions

Extentions for Partial Predication Support
- conditional move
    - register from the integer or floating-point register file is used to hold the condition rather than special register file
- select

Compiler Support

Compiler Support for Full Predication

- hyperblocks

Compiler Support for Partial Predication

- Predicate Promotion
  - removing the predicate from a predicated instruction
- Basic Conversion
  - replace each predicated instruction by a sequence of instructions with equivalent functionality
- Peephole Optimizations
  - ineficiencies since each instruction is considered independently

Results:

8-issue Processor 1 branch/cycle
Assuming 2-cycle branch prediction miss penalty

Conditional Move allows about 30% performance gain
Full Predication - another 30% gain over *conditional move*

6.893

“The Program Decision Logic Approach to Predicated Execution”

Serhii Zhak

10/26/2000

Architecture Support

Baseline Predicate Architecture
- PlayDoh is a EPIC architecture

Limitations of PlayDoh
- no convenient way to perform arbitrary logical operations on predicate register values: hurt Boolean minimization approach

Predicate Define Extensions

Overview of Compiler Techniques

- hyperblock

- predicate promotion

Minimization of Program Decision Logic

- Optimizations of predicate expressions
- Two-Level predicate synthesis
- Factorization

Results:

Program decision logic minimization provides an average over-all speedup of 13% for an 8-issue Processor