Alpha 21264 Microarchitecture

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21264 Overview

- 64-bit RISC Processor
- 500-1000 Mhz
- 7-stage pipeline
- 15 million transistors
- 2.2V, 60W
- 310 mm^2 (.35 micron)
- Target apps: Internet servers, data warehousing, digital video, speech recognition

21264 Fetch Unit

- 4 instructions/cycle, speculative
- Prediction:
  - Line/way predictor for each icache line (2-way, 64K)
  - 3 branch prediction mechanisms
    - Local: 2 level, 10-bit history pattern predictor (e.g. 10101010)
    - Global: History of last 12 branches, 4096 entry, 2-bit saturation
    - Chooser: Chooses between local/global
  - Prediction tables: **3.6KB**
  - Targets: **6KB**
  - 90-100% accurate on most benchmarks
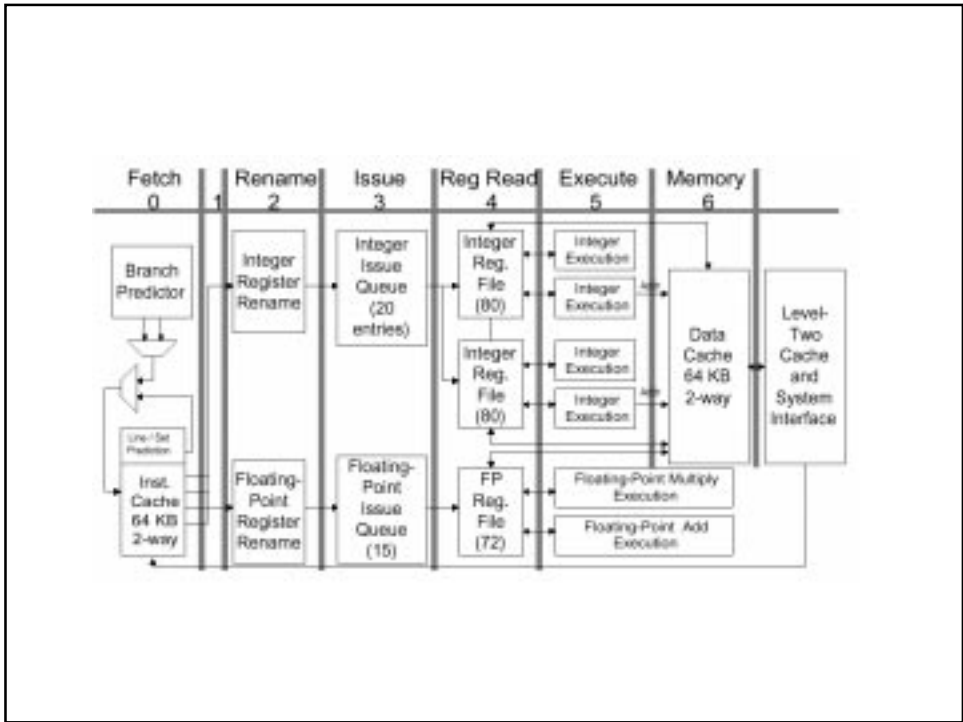
21264 Dispatch and Execution

- 4 integer execution units (2 clusters)
  - Each maintains copy of 80-entry register file
  - Single cycle latency for basic integer ops
  - Integer population count/leading zero count
  - Fully-pipelined multiplier
  - Motion Video Instructions (MVI)
- 2 FP execution units (1 cluster):
  - Upper: Multiply
  - Lower: Add, IEEE Divide, SQRT
  - 72-entry RF
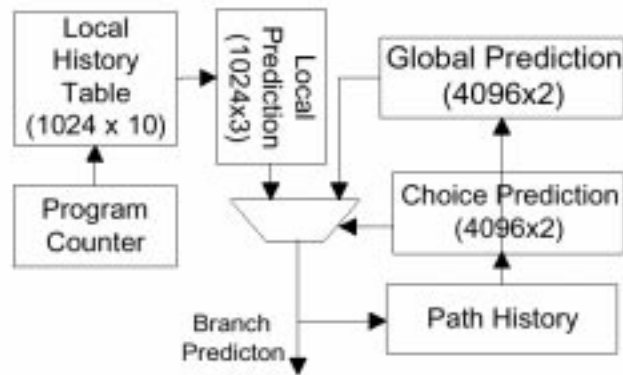
21264 Memory System

- 2, 64-bit data buses for icache/dcache
- 32 in-flight loads, 32 in-flight stores
- Dcache increased to 64K (2-way), double-pumped
- L2 Cache:
  - Moved off-chip (increased latency by 6)
  - 4 GB/s sustained bandwidth
- Speculative issue consumers of loads for 3 cycle integer load hit latency
- 1.3 GB/s sustained bandwidth on McCalpin Stream

Out-of-order execution

- User visible registers: 32 int/32 float
- Renaming registers: 41 int/41 float
- Renaming map data saved for precise exception handling
- 80 instruction in-flight window, in-order retirement
- Loads can speculatively bypass stores
  - Store wait bits for mis-speculation

Fetch Rename Issue Reg Read Execute Memory
0   1   2   3   4   5   6

Branch Predictor

Integer Register Rename

Integer Issue Queue (20 entries)

Integer Reg. File (80)

Integer Execution

Integer Execution

Integer Reg. File (80)

Integer Execution

Integer Execution

Data Cache 64 KB 2-way

Level-Two Cache and System Interface

Line-/Set Prediction

Inst. Cache 64 KB 2-way

Floating-Point Register Rename

Floating-Point Issue Queue (15)

FP Reg. File (72)

Floating-Point Multiply Execution

Floating-Point Add Execution

21264 Prediction Mechanisms

Local History Table (1024 x 10)

Local Prediction (1024x3)

Global Prediction (4096x2)

Program Counter

Choice Prediction (4096x2)

Branch Predicton

Path History

21264 Execution Units