## Power and Performance Analysis of PDA Architectures

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### Motivation

- Provide standard performance and power benchmarks for PDA architectures
- Run benchmarks on existing platforms and hypothesize areas of weakness

- Performance Benchmarks
  - Task switching
  - GUI window operations
  - JVM (SPECjvm98)
  - MPEG playback
- Power Analysis code sequences
  - Simple ALU operations
  - Memory Loads/Stores
  - Procedure call overhead
  - Branch Prediction

• Task Switching-

Enumerate through top ten window handles in the operating system queue.

Cycle 1000 times activating each handle and measure time to completion.

• GUI window operations-

Creation of single window with multiple MFC elements (command bar, text fields, label...etc).

Repositioned window forcing system to redraw 1000 times and measured time to completion. • JVM (SPECjvm98)

-jess: LISP like expert shell system

-jack: parser generator modeled after yac

-mpeg: MPEG layer-3 decoding

• MPEG playback

# Used PocketTV to play an MPEG clip (1.06MB).

Measured power and subjectively judged quality of playback.

• ALU Test-

Chose two distinct registers and performed addition, subtraction, and multiplication operations.

Measured power during loop of instructions.

• Memory Loads/Stores-

Read value from memory and write value back to same address. Ensures 100% cache hit.

Measured power during loop of instructions.

• Procedure Call Overhead-

Motivation: After looking at assembly code generated by GUI benchmarks, large percentage of instructions were related to operating system level or shared library call outs.

Called a procedure with four arguments. Action of procedure was to simply return.

Measured power during loop.

• Branch Prediction-

Randomly jump between 8 lines of code. After jumping program moves back to initial position through an unconditional branch.

Measured power during loop.

• Methodology for Power Measurement:

-Used lab power supply of 5.5 V

-Placed 1.26 ohm resistor in series with power supply, and measured voltage drop across it.



• PDA Overviews:

-Aero 2100 series:

MIPS4K Family, 70 Mhz

16 MB RAM

32 GP registers

8K direct mapped data cache (WB)

32-entry TLB (fully associative)

- PDA Overviews:
  - -Casio E-115:
    - MIPS4K Family, 131 Mhz
    - 32 MB RAM
    - 32 GP registers
    - 8K direct mapped data cache (WB)
    - 32-entry TLB (fully associative)

• PDA Overviews: -iPAQ H3600: Intel StrongARM SA-1100 series, 206Mhz 32 MB RAM 27 GP registers 8K 2-way set associative data cache (WB)2 32 entry fully associative TLB's

• PDA Overviews:

-Jornada 540 Series:

SH3 Processor, 133 Mhz

16 MB RAM

16 GP registers

8K 2-way set associative data cache (WB)

128 entry TLB (4-way set associative)

- Results
  - Performance Tests
  - General Power Measurements
  - Runtime Power Measurements
  - Architecture Power Measurements

#### **Power and Performance Analysis of PDA Architectures**



Poor performance on jack & mpeg:

- Require access to large input files

- Both performance tests scale proportionally per platform

- We therefore believe poor performance is due to slow memory access

## Poor performance on task switching: Possible causes:

 Proportionally smaller data cache as compared to other consumer level
CPU's such as desktop machines and laptops, which forces memory access.





General trends between platforms seem similar. Interesting observation: Aero and Jornada peak more on memory intensive tests.

> Both have 16 MB of RAM as opposed to 32 MB of iPAQ and Casio. Could be due to memory fragmentation.



## Conclusions

- Current PDAs suffer issues similar to issues in desktop and laptop computers (memory latency, data caching...)
- Particularly weak areas seem to be task switching and file I/O