

## Next Generation On-chip Communication Networks

### Project Members:

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### Project Goal:

Due to the constraints of VLSI scaling, future processor and system-on-chip designs will by necessity incorporate on-chip communication networks. In the project, we plan to investigate protocols and signalling technologies in the context of future on-chip multiprocessors in the 50nm regime. In this regime, interconnect delay becomes a major challenge and needs to be taken into account at all levels. This will require predicting scaling trends for devices and interconnect, and based on these models designing protocols and circuits. Our main design goal is minimum energy delay product.

### Plan of work:

Literature search - 10/10

Transistor modeling - 10/24 - Albert

Protocol design - 10/31- Jason  
RTL simulation - 11/28

Driver/Repeater/Receiver - Seongmoo  
Initial Circuit designs - 11/8  
Initial layouts - 11/8  
Final Circuit design - 11/28  
Final Layout - 11/28

Crossbar - Albert  
Initial Circuit designs - 11/8  
Initial layouts - 11/8  
Circuit design - 11/28  
Layout - 11/28

### Tools/Infrastructure:

Xcircuit, Magic, Space, HSpice, TimeMill, PathMill, PowerMill, VCS