Kenneth Barr
Kenneth Conley
Serhii Zhak

“Correlation Between State and Control Signals in Out-of-Order Issue Logic” Project Proposal

Out-of-order issue logic is getting more complex and increasing in its usage of on-chip power. Current out-of-order logic is optimized for performance and does not take advantage of current power-saving techniques. We propose to examine the key out-of-order logic structures, including the register renaming logic and superscalar issue logic, in order to determine what power-saving techniques can be applied. We plan to pay close attention to predictive and memoization techniques.

As part of our study, we will look for correlation between state and asserted control signals. We will do this by using a superscalar microprocessor simulator, such as SimpleScalar, to run common benchmarks. We will add analysis routines to collect key data in the renaming and issue logic stages.

We will also attempt to redesign logical structures to increase the correlation between these signals. We will then implement these new logical structures in our simulator and determine the performance trade-off for these optimizations.

Time permitting, we will try to determine the best logical structures that can be implemented that will allow predictive and/or memoization techniques to be applied to the out-of-order logic. These will also be implemented in our simulator, and we will try to create a model to measure the performance and power trade-offs of our final design.

Several key issues will have to be resolved in this study. We will need to determine what kind of mispredictions are possible in our scheme, as well as determine how to detect these mispredictions. Also, we will have to develop a model to determine the power savings of our new implementation offers.