Alpha 21264: Microarchitecture and Performance

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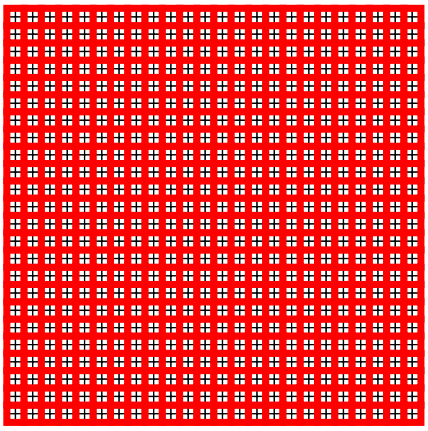
http://www.cag.lcs.mit.edu/6.893-f2000/

35nm Chip



- Each red square has edges one clock cycle long
- Finer grid is tiles with half-perimeter of one clock cycle
- Assumes 8 FO4 cycle, 30mm chip edge

Next Few Weeks

- **9/19 T *Alpha 21264* case study part 2: VLSI Implementation**
  gronowski:ijssc:1998 (Albert Ma),
  farrel:jssc:1998 (Mike Zhang)
- **9/21 R Limits of conventional microarchitecture scaling**
  palacharla:isca:1997(?),
  agarwal:isca:2000(?)
- **9/26 T Project proposal**
  written proposal + class presentation
- **9/28 R Low Power Design**
  Lecture
- **10/3 T Parallel Architecture Overview**
  Lecture