Integrated Circuit Optimization by Means of Evolutionary Multi-Objective Optimization

Matthias Blesken
System and Circuit
Technology
University of Paderborn,
Germany
blesken@hni.uni-
paderborn.de

Anouar Chebil
System and Circuit
Technology
University of Paderborn,
Germany
anouar@hni.uni-
paderborn.de

Ulrich Rückert
Cognitronics and Sensor
Systems
University of Bielefeld,
Germany
rueckert@cit-ec.uni-
bielefeld.de

Xavier Esquivel
Computer Science
Department
CINVESTAV-IPN, Mexico
esquivel@cs.cinvestav.mx

Oliver Schütze
Computer Science
Department
CINVESTAV-IPN, Mexico
schuetze@cs.cinvestav.mx

ABSTRACT

The design of resource efficient integrated circuits (ICs) requires solving a minimization problem which consists of more than one objective given as measures of the available resources. This multi-objective optimization problem (MOP) can be solved on the smallest unit of the IC, the standard cells, to improve the performance of the entire circuit.
In this work, transistor sizing of an IC is approached via a multi-objective approach which includes the use of multi-objective evolutionary algorithms (MOEAs). We compare the performance of two MOEAs on a four-dimensional MOP of a particular standard cell. The results indicate that evolutionary strategies are suitable for the treatment of such problems and advantageous against other rather classical methods.

Categories and Subject Descriptors

G.1.6 [**Optimization**]: Global Optimization; D.2.8 [**Software Engineering**]: Metrics—*complexity measures, performance measures*; B.7.1 [**Integrated circuits**]: Standard cells

General Terms

Design, Performance

Keywords

multi-objective optimization, evolutionary computation, circuit design, CMOS standard cells.

1. INTRODUCTION

A resource efficient design of standard cells is the basis for a resulting resource efficient design of the integrated systems (e.g., [1, 2]). That is, improvements on the smallest unit will affect positively the overall performance of the entire IC. Optimization of standard cells is basically the search for 'optimal' transistor sizes since the transistors' widths and lengths influence significantly the consumption of the circuit resources. Important characteristics of logic gates are noise margins as well as time and power dissipation. Hence, a multi-objective optimization problem (MOP) arises naturally when stating the sizing problem of CMOS standard cells. Apparently, the multi-objective approach, i.e., the computation/approximation of the entire solution set (the Pareto set), takes these objectives directly into account. Here we address the problem of designing optimal ICs by means of evolutionary computation.
On the examples of several CMOS gates we demonstrate in this work that the well-known MOEAs SPEA ([16]) and the ϵ-MOEA ([10]) can be successfully applied to optimize standard cells. For gates representing logic functions with even quite a few boolean variables deterministic search algorithms collapse due to the relatively high computational cost for a performance evaluation. In those cases the two MOEAs under consideration still compute sufficiently good results which we show on the And-Or-Invert gate. This is a four dimensional example where both MOEAs succeed while another (classical) method reaches its limit.

The remainder of this paper is organized as follows: In Section 2, we present the background and related work. In Section 3, we introduce how a MOP for the design of standard cells is deducted from a gate's circuit properties using the example of an inverter. In Section 4, we present some numerical results comparing two MOEAs performing on a more complex CMOS standard cell. In Section 5, we address a sensitivity based decision support of this application, and finally, we conclude in Section 6.

2. BACKGROUND AND RELATED WORK

A multi-objective optimization problem (MOP) can be stated as follows:

$$\min_{x \in R} F(x), \qquad (1)$$

where $F : R \subset \mathbb{R}^n \to \mathbb{R}^k$ is defined as the vector of k objective functions $f_i : R \subset \mathbb{R}^n \to \mathbb{R}$, $i = 1, \ldots, k$, and where R is the restriction set

$$R = \{x \in \mathbb{R}^n \ : \ g(x) \le 0 \text{ and } h(x) = 0\}, \qquad (2)$$

where $g : \mathbb{R}^n \to \mathbb{R}^m$ and $h : \mathbb{R}^n \to \mathbb{R}^p$ are the mappings defining the inequality and equality constraints, respectively. A point $x \in R$ is said to dominate an other point $y \in R$ (in short $x \prec y$), if $f_i(x) \le f_i(y)$ for all $i \in \{1, \ldots, k\}$, and if there exists an index $j \in \{1, \ldots, k\}$ such that $f_j(x) < f_j(y)$. A point $x \in R$ is called optimal, or *Pareto* optimal, with respect to (1), if there is no other point $y \in R$ that dominates x. The set $\mathcal{P}$ of all optimal solutions is called the Pareto set, and its image $F(\mathcal{P})$ is called the Pareto front.

So far, there exists a huge variety of methods for the computation of the Pareto set of a MOP. Among them, multi-objective evolutionary algorithms (MOEAs) have caught the attraction of many researchers (e.g., [7, 6] and references therein). One major reason for this might be that the population based approach together with a stochastic component in the search procedure allows typically for an approximation of the entire (global) Pareto set in one single run of the algorithm. This represents an adantage over most mathematical programming techniques, which require in addition certain smoothness assumptions on the MOP.
Multi-objective approaches to design integrated circuits (however, different than the ones considered in this paper) can be found in the works of Dienstuhl [11] and Thomas [14]. Both authors applied and adjusted the SPEA to optimize memory elements [11] and adders [14] for timing, resistance, power consumption and chip area. In [3], the search for optimal transistor sizings of standard cells was performed by the software tool GAIO[1]. A whole new standard cell library for sub-threshold operation was designed based on a multi-objective approach and supported by SPEA as documented in [2].
Earlier algorithmic optimization approaches for integrated circuit design are, most likely due to less available computation power, single objective approaches. Although Fischer et al. [12] do not explicitly formulate it, they transform the problem into a scalar objective optimization problem. They developed several algorithms to minimize resources as power, speed and silicon area in one objective while restricting the other resources by an upper bound. Borah et al. [4] minimize power while constraining the delay time.

For the treatment of the MOPs at hand we have chosen to take and compare two different MOEAs. First, we have chosen for SPEA since this algorithm has already been used successfully for the design of integrated circuits. Second, we have chosen for a variant[2] of ϵ-MOEA which is a steady state MOEA and which offers certain convergence properties

[1] Global Analysis of Invariant Objects, see www.math.upb.de/~agdellnitz
[2] The name of this algorithm is not given here for sake of a bouble blind review.

for the limit set of the external archive of the MOEA (e.g., [13]).
To compare our results we use the Hausdorff distance to measure the distance between the the final population and the Pareto set as well as the indicator Δ_p which which is a composition of the Generational Distance (GD, see [15]) and the Inverted Generational Distance (IGD, see [5]).

Definition 2.1 *Let $u, v \in \mathbb{R}^n$, $A, B \subset \mathbb{R}^n$, and $\| \cdot \|$ be a vector norm. The* Hausdorff distance $d_H(\cdot, \cdot)$ *is defined as follows:*

(a) $dist(u, A) := \inf_{v \in A} \|u - v\|$

(b) $dist(B, A) := \sup_{u \in B} dist(u, A)$

(c) $d_H(A, B) := \max(dist(A, B), dist(B, A))$

Definition 2.2 *Let $X = \{x_1, \ldots, x_n\} \subset \mathbb{R}^n$ be a candidate set and $Y = \{y_1, \ldots, y_n\} \subset \mathbb{R}^k$ be its image, i.e., $y_i = F(x_i)$, $i = 1, \ldots, n$. Further, let $\mathcal{P} := \{p_1, \ldots, p_m\} \subset \mathbb{R}^k$ be a discretization of the Pareto front. Then it is*

$$\Delta_p(Y, \mathcal{P}) =$$
$$\max \left(\left(\frac{1}{n} \sum_{i=1}^{n} dist(y_i, \mathcal{P})^p \right)^{1/p}, \left(\frac{1}{m} \sum_{i=1}^{m} dist(p_i, Y)^p \right)^{1/p} \right) \qquad (3)$$

It is $\Delta_\infty = d_H$, but for finite values of p the indicator Δ_p averages (using the p-vector norm) the distances considered in d_H. Hence, in spite of d_H, Δ_p does in particular not punish single (or few) outliers in a candidate set.

3. SIZING A CMOS INVERTER USING MOEA

Figure 1 shows the netlist of a simple electric circuit containing two metal-oxide-semiconductor field-effect transistors (MOSFETs) T1 and T2. V_{dd} denotes the supply voltage which is the highest potential in the circuit. A MOSFET can be thought of as a voltage controlled resistor. Both transistors are of different types. T1 is a pMOSFET (indicated by the ring) whose resistance decreases with decreasing gate-source voltage $V_{\mathrm{in}} - V_{\mathrm{dd}}$ (which is always negative). T2 is an nMOSFET (without ring) whose resistance decreases with increasing gate-source voltage[3] V_{in}. Thus, the output voltage V_{out} is pulled up when the input voltage V_{in} drops and falls if V_{in} rises. Because a logic '1' is mapped to a logic '0' and a '0' to a '1' this circuit is an inverter and due to the transistor types it is built with a so-called CMOS inverter (CMOS, Complementary Metal Oxide Semiconductor). Given an alternating input signal the resulting output signal will not be a perfect inversion of the analog signal. Figure 2 shows an example of a possible input/output relation. Particularly there is always a delay which can be measured as the timespan between both signals crossing $50\% V_{\mathrm{dd}}$ indicated by $t_{\mathrm{pd,HL}}$ and $t_{\mathrm{pd,LH}}$. One objective in designing an inverter is thus to minimize

$$t_{\mathrm{pd}} = \max\left(t_{\mathrm{pd,HL}}, t_{\mathrm{pd,LH}}\right). \qquad (4)$$

The circuit's switching properties can be influenced by the

[3] The position of a transistor's source contact depends on its type. The nMOSFET's source is here connected to ground and the source of the pMOSFET T1 is connected to V_{dd}.
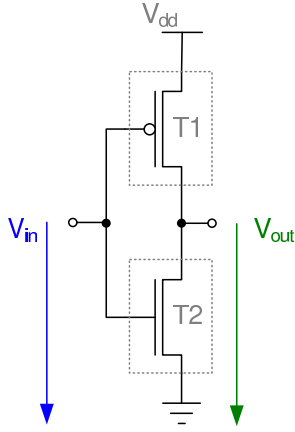
Figure 1: Netlist of the CMOS inverter

Figure 3: DC signal input V_{in} to output V_{out}.

designer when sizing the transistors. For each transistor a width and a length can be chosen. These parameters control the current flow through the transistor's channel. The length is usually set to a minimal size to attain low area consumption. A wider transistor has less resistance than a device of smaller width. Therefore, a circuit can be sped up by increasing the width of its transistors which leads in turn to a reduction of the delay time t_{pd}.

Increased current floating from V_{dd} to ground on the other hand means that more energy E_{dyn} is consumed. Larger transistors create larger parasitic capacities that have to be charged for switching the output which also raises energy consumption induced by current from the input E_{in}. Hence, a second important objective to be minimized is

$$E = E_{dyn} + E_{in} \tag{5}$$

In digital integrated circuit design standard cells representing simple logic functions like an inverter, NAND or NOR are connected to build more complex functions. Here it has to be secured that the logic value of one output signal is interpreted by the next cell's input as the right value. With

$$NM = \min(NM_H, NM_L) \tag{6}$$

where

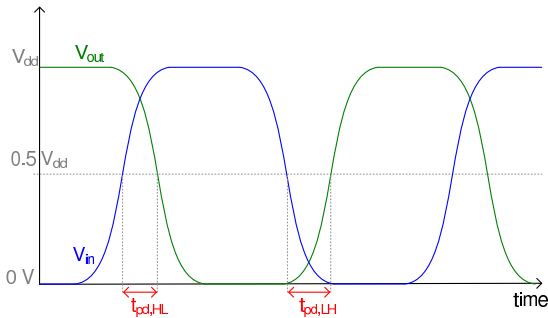$$\begin{aligned} NM_H &= |U_{OH} - U_{IH}| \\ NM_L &= |U_{IL} - U_{OL}| \end{aligned} \tag{7}$$

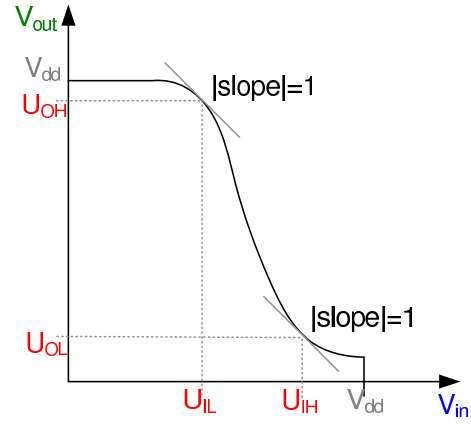**Figure 2: Transient signal input V_{in} and output V_{out}.**

a safety (or noise) margin the NM is defined to measure a standard cells robustness towards noise that could lead to misinterpretation of the logic levels. $U_{IL}, U_{IH}, U_{OL}, U_{OH}$ are defined as indicated in Figure 3. The noise margin should be maximized.

A MOP which naturally arises for the CMOS standard cells hence reads as follows:

$$\min_{x \in R} \{-NM, t_{pd}, E\} \tag{8}$$

where R is the search space spanned by the n transistors' widths W_1, ..., W_n. The lower bound for each width is usually given by a minimal possible width. For the 65 nm technology this is 0.12 μm. The designer will also define an upper bound based on the application. Thus, R is connected and compact as it is defined by box-constraints.

As described in [1] the relation between the widths of the pMOSFET W_1 and the nMOSFET W_2 should be

$$W_1 = \alpha \cdot W_2 \tag{9}$$

where $\alpha \approx \frac{\mu_p}{\mu_n}$ and μ_p and μ_n are constants of the mobility of holes and electrons, respectively. The approximation of (9) aims for symetric input-output-curve and thus inderectly achieves decent noise margins and delay times. In [3], this procedure is described as the classical approach. The advantage is that for a given driving strength all parameters are determined. For more complex CMOS logic gates the widths of all pMOS- and nMOS-transistors have to be summarrized. The disadvantage is that this approach limits the designer's freedom in optimizing the circuit properties directly. An exploration of the complete search space supports the designer with all resource efficient designs that he/she could choose from. Very often the direct approach finds designs that dominate the ones that would be computed based on the classical approach [3].

Figure 4 shows an approximation of the Pareto set and front of MOP (8) for the CMOS inverter. It can be seen that a major part of the Pareto set indeed satisfies the linear relationship given in Equation (9). The set opens conical with larger transistor widths which is because the noise margin and delay times are less conflicting at smaller transistor widths. The buckle in the Pareto set is due the box-constraints: When the minimal value of W_2 is reached, W_1 can still be reduced which lowers energy consuption E and
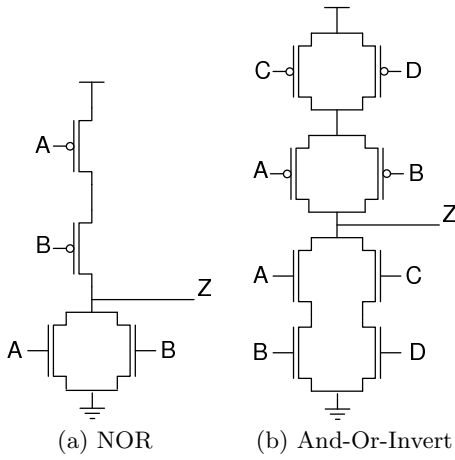
Figure 5: Schematics of CMOS gates.

Figure 6: Approximated Pareto front of the MOP (8) for the And-Or-Invert gate schown in Figure 5.

decreases t_{pd} and -NM at the same time. Since two out of three objectives are not conflicting in this area its image resembles a one-dimensional set.

4. OPTIMIZATION TECHNIQUES FOR SIZING CMOS STANDARD CELLS

Using both nMOSFET and pMOSFET more complex logic gates than the inverter can be assembled. A CMOS circuit consists of a *pull down path* of nMOS transistors that can pull down the voltage of the output vertex Z to ground and pMOS transistors buliding a *pull up path* to eventually pull up the Z to the supply voltage V_{dd}. The number of the nMOSFETs and pMOSFETs are equal. Parallel transistors of the pull up path appear in the pull down path connected in series with the same input signals connected to their gate contact. As a consequence the output Z never has a high impedance meaning that its digital value is always either zero or one. The way CMOS logic gates are constructed it is easier to build circuits of logic expressions that contain an inversion. Figure 5 shows the schematics or netlists of an inverted Or gate called *NOR* ($Z = \overline{A \vee B}$) and an *And-Or-Invert AOI* ($Z = \overline{(A \wedge B) \vee (C \wedge D)}$). In inverting CMOS gates the minimal number of transistors is twice the number of boolean parameters. Some transistors can and should be sized equally but in general the complexity of the search space of the sizing promblem R rises with the number of input signals. Hence, for the NOR gate R can be two-dimensional spanned by all nMOS and pMOS transistors' widths W_{n} and W_{p}, respectively. The result of the Pareto optimization for this search (including additional information, see Section 5) is shown in Figure 7.

There is an advantage of expending R to a third dimension allowing both pMOSFET's widths to be chosen independently. The possible gain is documented in [3]. There the Pareto set was approximated by subdivision techniques and thus the extension of the search space resulted in a massive runtime increase. For a worst case scenario the runtime depends exponentially on the number of dimensions of R. As a consequence, when facing the optimization problem of more complex gates like the AOI, new search strategies which can cope with larger search spaces have to be used.
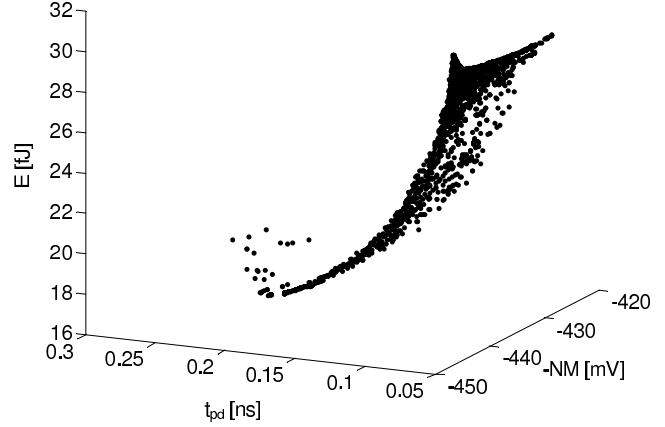
Here, we have chosen for an AOI consisting of four variables[4]. This is a good example to compare different evolutionary strategies for the application of sizing integrated circuits.

On the one hand, we used the Strength Pareto EA (*SPEA*). It uses the concept of Pareto dominance to assign *fitness values* for the tournament to each *individual* of a *population*. In our implementation we use a polynomial mutation (PM) as introduced in [9] where each individual is set off by a random variable with a parameter controlled variance. The *crossover* is derived from the *simulated binary crossover* (SBX) introduced in [8]: For every randomly chosen pair of individuals (*parents*) two *children* are generated such that the parents' barycenter stays the same for the children.

On the other hand, we have used ϵ-MOEA equipped with PM and SBX. Since the objectives in MOP (8) have been evaluated by a simulator which requires certain (significant) time to initialize and free the required memory, we have selected in each iteration step $2 * N_{iter}$ parents for the generational operators.

Table 1 shows some numerical results for the AOI gate obtained by SPEA and ϵ-MOEA. Here, we have chosen a budget of $N_1 = 1700$ and $N_2 = 4000$ function evaluations per run of the algorithm. For N_1, the computational time for one run for both algorithms was approximately one hour, and more than two hours for N_2. For the plot of the Pareto front see Figure 6. As reference solution we have taken the results of much longer runs (one from each MOEA). The results show that i) there is no clear winner out of the two competitors though there is a slight advantage for SPEA, and ii) that both MOEAs are capable of producing satisfying results in this application since a maximal error (obtained by discretization or by lack of convergence) of 0.3 is still acceptable for the AOI gate under consideration.

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[4]These are the widths of the left transistors of the schematic in Figure 5(b). The right transistors are sized equally.
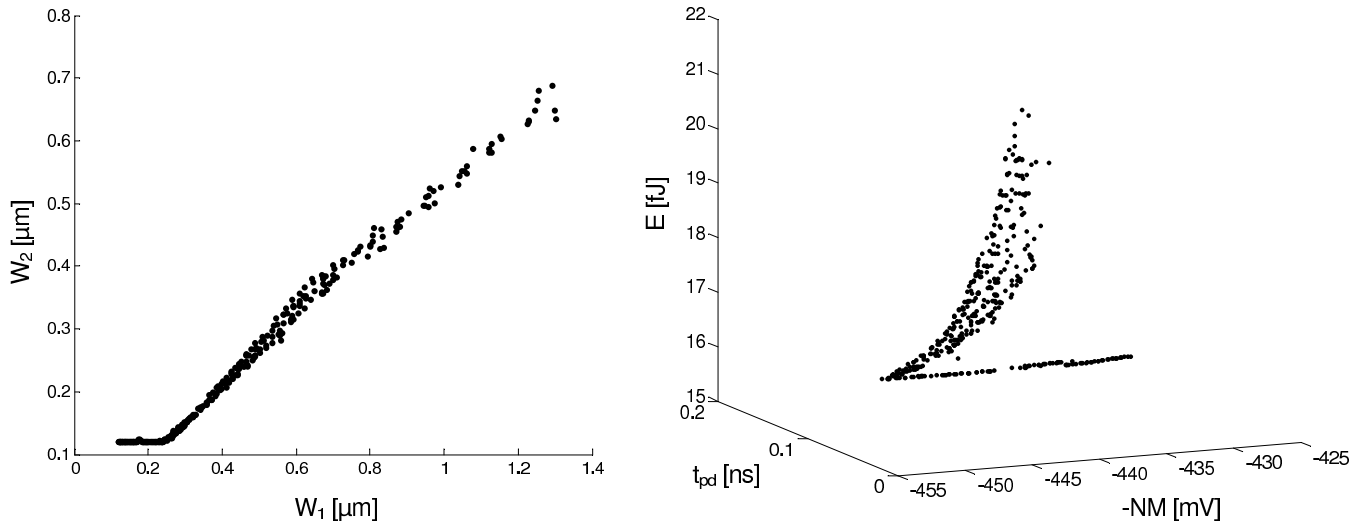
Figure 4: Approximated Pareto set and front of the MOP (8) for the CMOS inverter shown in Figure 1.

Table 1: Numerical results for SPEA and ϵ-MOEA for the AOI gate. The results are averaged over 10 independent runs.

	$N_1 = 1700$			$N_2 = 4000$		
	Δ_1	Δ_2	d_H	Δ_1	Δ_2	d_H
SPEA	0.134	0.216	0.271	0.083	0.094	0.257
ϵ-MOEA	0.111	0.123	0.248	0.132	0.142	0.287

5. DECISION SUPPORT

The design process of logic gates requires choosing transistor sizes such that the corresponding circuit properties result in a tradeoff between several resources. The search algorithms support the designer of an integrated circuit with the set of all resource efficient sizings thus providing a great variety of choices.

All simulations for the search have been performed based on average values for parameters of the circuit's environment such as temperature and supply voltage. But these values can vary and thus as part of the design process sensitivity of the circuit has to be analyzed and reduced.
A measure of sensitivity in one particular objective can support the designer in choosing elements from the set of resource efficient sizings. Figure 7 shows the Pareto set of the CMOS NOR gate with grey shades indicating the sensitivity of the objectives NM, t_{pd} and E. This is a simple example to indicate the idea of sensitivity based decision support on an example of a two-dimensional search space. For the four-dimensional AOI gate a visualization is not as easy anymore and thus not presented here. Also measures combining several objectives' sensitivities can be defined and thus simplify even more complex dependencies.

6. CONCLUSIONS AND FUTURE WORK

We showed that a MOP naturally arises when stating the sizing problem of CMOS standard cells. With examples of several CMOS gates we demonstrated that the SPEA and the ϵ-MOEA can be successfully applied to optimize standard cells. For gates representing logic functions of many boolean variables search spaces are higher dimensional and deterministic search algorithms collapse. In those cases MOEAs still provide sufficient results which was demonstrated on the And-Or-Invert gate. This four-dimensional example's Pareto set was approximated by the ϵ-MOEA with similar precision as the SPEA.

We introduced a simple example of a NOR gate to visualize the possibility of using sensitivity measures for decision support (see Figure 7). Here it could be discovered that larger transistors are less sensitive which is in general expected (however, not to which extend). This dependency is not guaranteed when gates become more complex. Sensitivity is especially difficult to predict and thus even more important to consider for analog circuits.

To support the designer in choosing robust elements from the set of resource efficient sizings of analog designs sensitivity measures are inevitable. For the search space exploration of such circuits it would even make sense to integrate such measures in the search process. This further increases the search space's complexity. So for these applications the MOEAs advantages over the subdivision techniques will increase even more.

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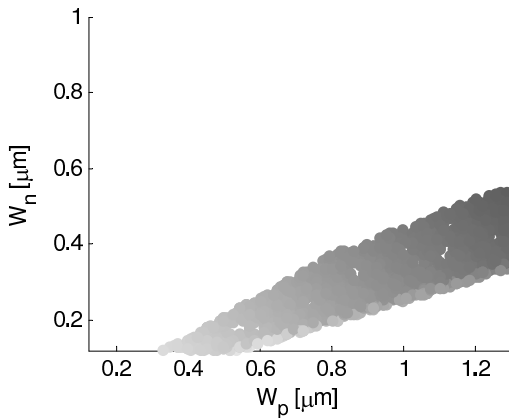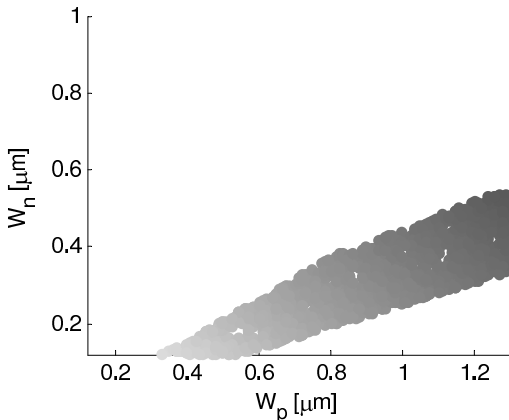
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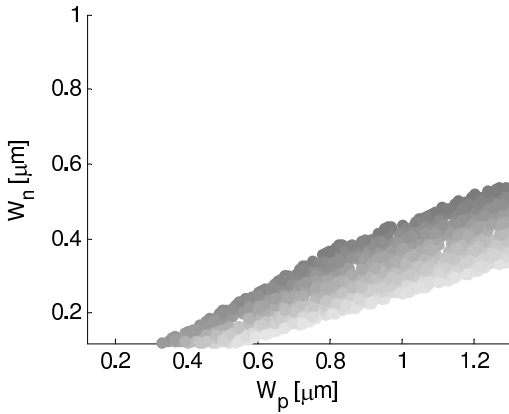
(a) Sensitivity of NM

(b) Sensitivity of t_{pd}

(c) Sensitivity of E

Figure 7: Pareto set of the CMOS NOR gate. Lighter grey shades indicate higher sensitivity of the objective towards variations in temperature or supply voltage than darker grey shades.

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