# Architecture Exploration and Performance Verification Environments for a Multi-Core Embedded SOC Platform Design

Gi-Ho Park, Hyun-Min Kyung, Jung-Bin Im, WooKyeong Jeong, Chang-Hoon Oh, Se-Hyun Yang, Kyoung-Soo Kim, Han-Jong Kim, Heung-Chul Oh, Tae-Jin Kim, and Sung-Bae Park

Processor Architecture Lab, SOC R & D Center, System LSI Division, Semiconductor Business Yongin-City, Kyeonggi-Do, Korea

## 1 SAViT (Standard/Synegistic/Superior Architecture for Versatile information Technology) Multimedia Platform

We are currently developing a mobile multimedia platform SOC named SAViT (Standard/Synegistic/Superior Architecture for Versatile information Technology) platform. This platform SOC has a heterogeneous multi-processor architecture with an ARM CPU (Central Processing Unit) and a StarCore DSP (Digital Signal Processor). The major target application of this platform is multimedia processing such as multiple format codec processing such as H.264, MPEG-4, and WMV-9. This platform is targeting the corporate level standard platform of Samsung Electronics, like OMAP for TI and PCA platform for Intel.

## 2 Architectural Exploration and Performance Verification

As the advance of process technology, tens of million gates can be integrated into a single SOC (System On a Chip) for embedded applications. We are expecting our first version of the SAViT platform for the mobile multimedia application will integrate more than 10 million gate on a chip. Architectural exploration and performance verification of this SOC is essential in designing this kind of complex chip. Various level of performance simulator environments enable the exploration of design alternatives for the complex SOC design.

We are building various level of architectural exploration and performance verification environments as follows including an FPGA board platform.

1. System level simulation environment: we have built a system level architectural exploration and performance verification environment based on ARM RealView MaxSim tool[1] as shown in Fig. 1. This platform environment has following components and it can run MPEG-4 decoder software.
   - Processor components: ARM1176 CPU + SC1400 DSP

  - System peripherals : memory system (DRAM/SRAM), DMA controller, AHB system bus, dynamic memory controller, static memory controller, etc.
  - Display related modules : LCD controller, post-processor, etc.
  - Simulation speed : between 10Kcycle/sec to 100Kcycle/sec based on the configuration.
2. Platform FPGA Board : we built a platform FPGA board to perform performance verification with a realistic image size and number of frames as shown in Fig. 2. The configuration of the FPGA board is as follows. It has two daughter boards for each processor. It can run an MPEG-4 decoder software and display the output to LCD similar to the system level simulation environment.
  - ARM11[2] Board: ARM1136 CPU testchip
  - StarCore[3] Board: SC2400 testchip + 4M/6M/8M gate FPGA
  - FPGA mother board: CPU interface, DSP interface, two 8M gate FPGAs, SDRAM/DDR, memory port for OneNand memory, 2.2" LCD, SD, Sim Card, Keypad, Modem, etc.
  - AHB bus, Static memory controller, dynamic memory controller, UART, LCD controller, post-processor in FPGA.
  - Simulation speed : around 20Mcycle/sec based on the configuration.
3. Hardware emulation : we are currently considering the use of hardware emulator like Cadence Palladium[4].
4. Chip board : we will develop chip board similar to the FPGA board with real SOC chip rather than FPGA. It will be used to check the real performance of the SOC chip and to develop software for the chip.

## 3 Plan for Architectural Exploration and Performance Verification

We will use the system level simulation environment for the architectural exploration for our platform SOC design. We will use the MaxSim environment to determine major architecture design, such as bus architecture, memory system architecture, etc. This is because the system level simulation environment gives the flexibility to explore large design space. The platform FPGA board will be used to check the efficiency of the architecture determined by the system level simulation environment with large data set based on the high speed of the FPGA board.

For the checking of the accuracy for these architectural exploration environment, we will compare and correlate the result of these simulation environment with that of real chip board. The chip will be fabricated in 90nm process and we are expecting that the SOC chip will be available in the end of this year.

## References

1. ARM, SOC designer with MaxSim Technology, information available at www.arm/com/products/DevTools/MaxSim.html

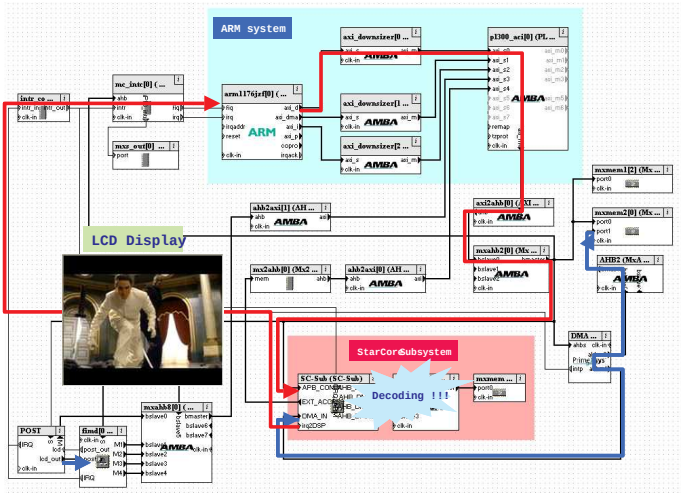


**Fig. 1.** System level simulation environment based on ARM RealView MaxSim Tool

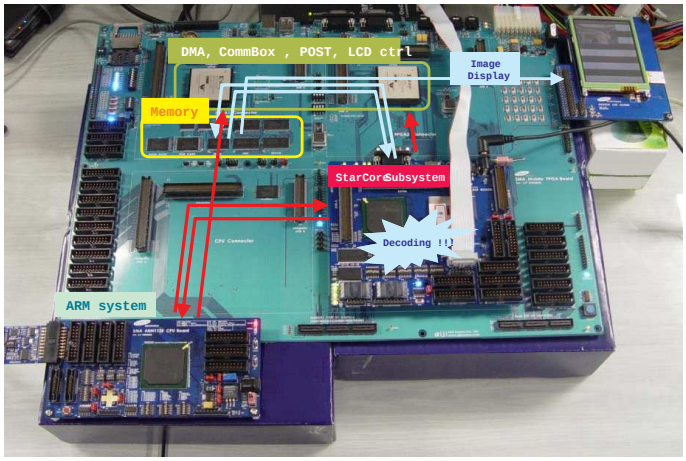


**Fig. 2.** Platform FPGA board (ARM11 + SC2400 DSP)

2. ARM, ARM1136JF-S and ARM1136J-Stm Technical Reference Manual, r0p2, ARM DDI 0211D, 2003. 8
3. StarCore LLC, SC1000-Family Processor Core Reference Manual, June 2004
4. Cadence Design Systems, Inc., Palladium QEL Reference Manual, Product Version 1.1.1 QSR3, January 2004