Architectural Exploration and Performance Verification Environments for a Multi-Core Embedded SOC Platform Design

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Samsung Electronics
SAViT Platform

Standard Synergy Superior
Architecture for
Versatile [Mobile/Personal/Home/Network]
information
Technology

☐ Save it!
Save Power and Cost
Save IT Industry with New Light

☐ Heterogeneous multi-processor Architecture with ARM CPU + StarCore DSP for Multimedia Processing
Platform (CPU + DSP) FPGA Board

DMA, CommBox, POST, LCD ctrl
Decoded data transfer

Display Image
DMA setting

Memory
Encoded data transfer

ARM ⇔ StarCore Communication
POST setting

ARM system

StarCore Subsystem
Decoding !!!
ARM1136 CPU Board

- ARM1136 Testchip ARM AHB signals are connected to SMA FPGA.
- ARM clock is bypassed.
StarCore DSP Board

- TC1202A or TC1402A Testchip
- 4M/6M/8M FPGA
Platform FPGA Board

SMA FPGA Board

- CPU I/F + DSP I/F + FPGA #1 + FPGA #2
- 8M gate FPGA #1 : CPU I/F + System Bus + UART + LCD
- 8M gate FPGA #2 : DSP I/F + User Defined Block
- Allow board stacking for Multi-CPU and Multi-DSP extension
- NOR, SRAM, SDRAM, DDR, (in Board), and Ext. port for OneNAND
- 2.2” LCD, SD, Sim Card, Keypad, Modem, etc
Platform (ARM1176 + SC1400) Virtual Platform

StarCore <-> ARM Comm.

Decoding !!!