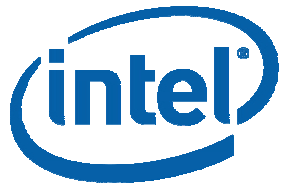

Clock control, interface and debug mechanism for an FPGA based x86 multi-processor emulator

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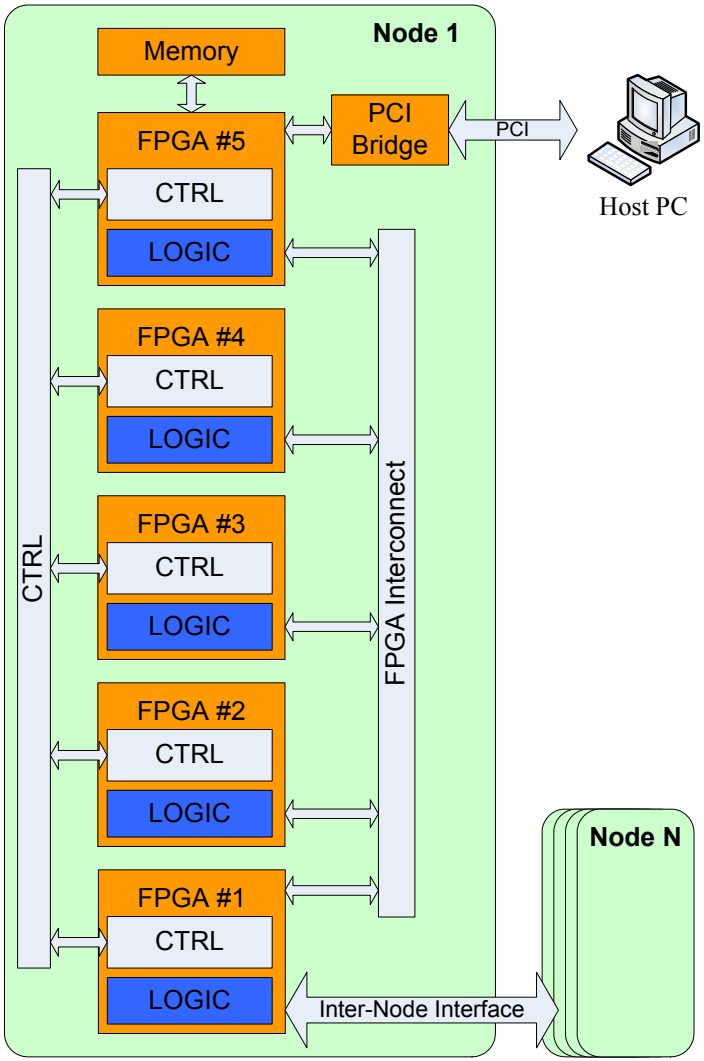
Motivation

- Get a cycle accurate simulation platform to investigate and study new architectural approaches in advance to silicon
  - Proof of concept
  - Comparison of different architectural approaches
  - System performance prediction of final silicon
- Improved performance over of-the-shelf prototype platforms and emulators
- Capabilities to debug design errors and to bring-up the emulated system
- Non intrusive performance measurements of the emulated system

Key features of the system

- Scalable, globally synchronous, system based on basic node cards
- System topology configured by pluggable high-speed serial board interconnects
- Fully controllable application clock
  - Single clock stepping mode
  - Stepping for predefined number of clock cycles
  - Continuous mode
  - Stop on event
- Tracing of emulated signals (e.g. busses, registers)
  - Performance optimized sampling of predefined signals
  - Full read-back functionality to capture "complete" state of the system
- TDM interfaces between FPGAs on one node card and between node cards
- Application frequency in the area of 20-30 MHz

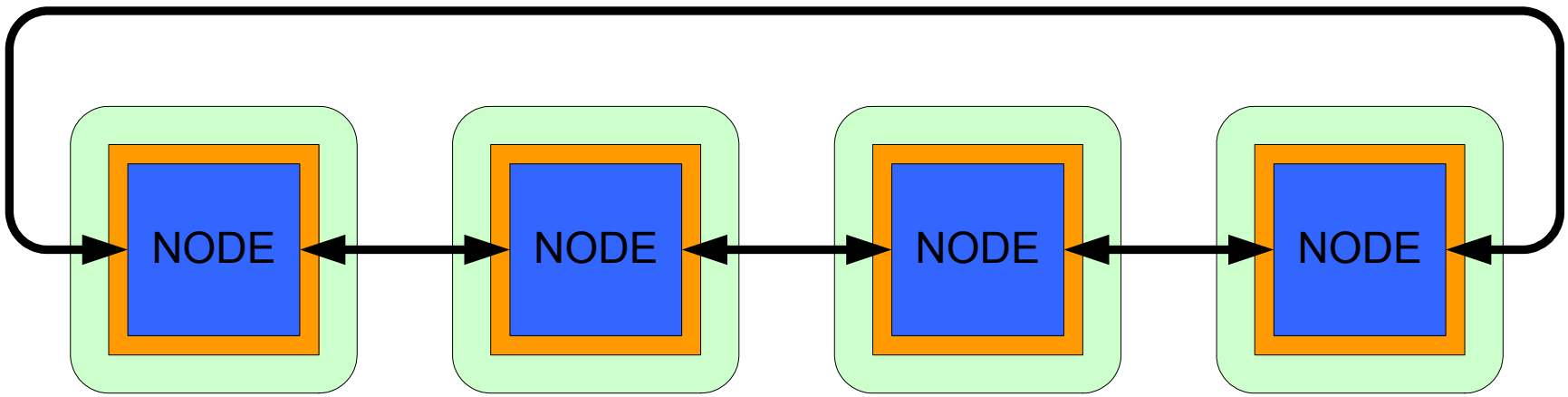
Basic Element: Node Card



- 5 Xilinx Virtex4 LX/FX FPGAs
- Up to 1GB memory provided for application
- Fixed physical interconnect topology
- Control and Debug via PCI interface
- Application (FPGA bit files and SW) loaded via PCI interface
- Scalable multi node system via RocketIO links (24 In / 24 Out)

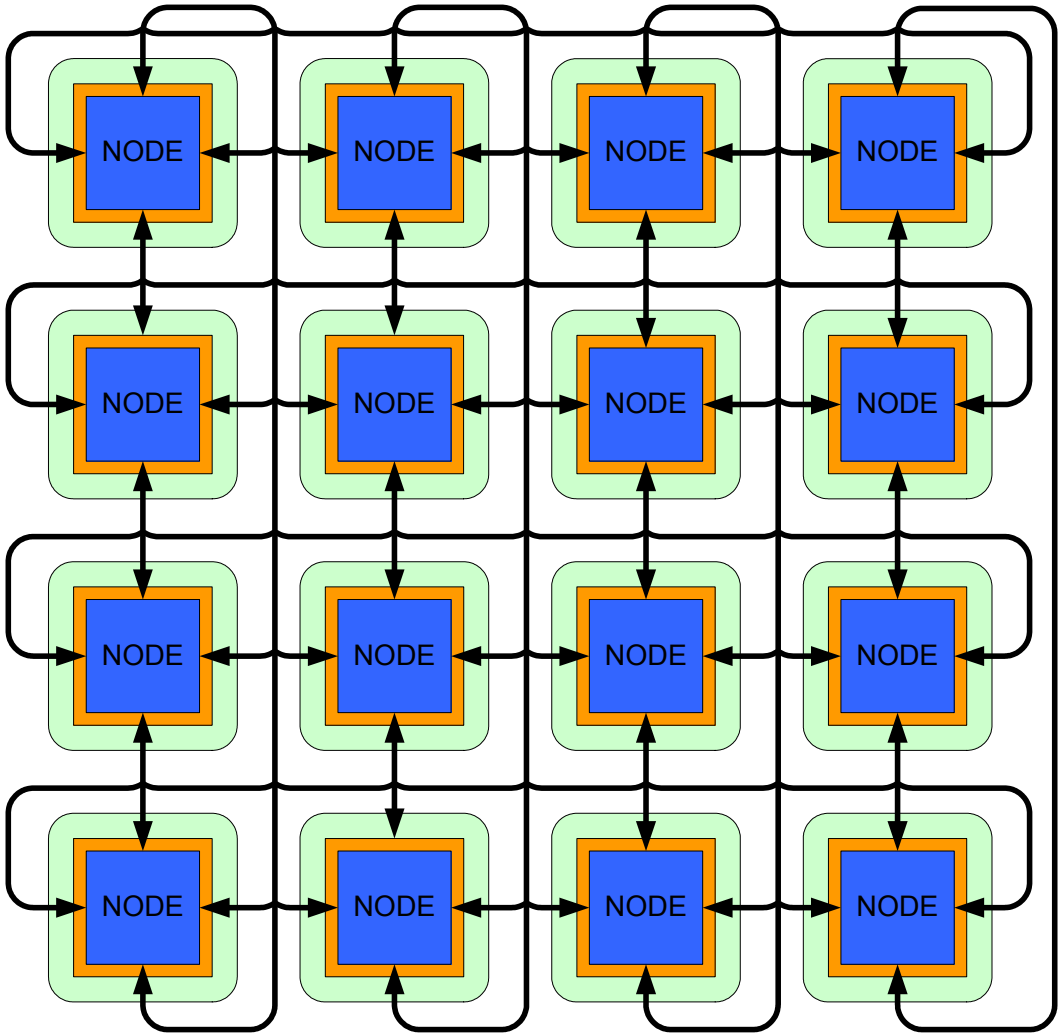
System Examples

- Ring architecture
- 12 RocketIO links to each neighbor



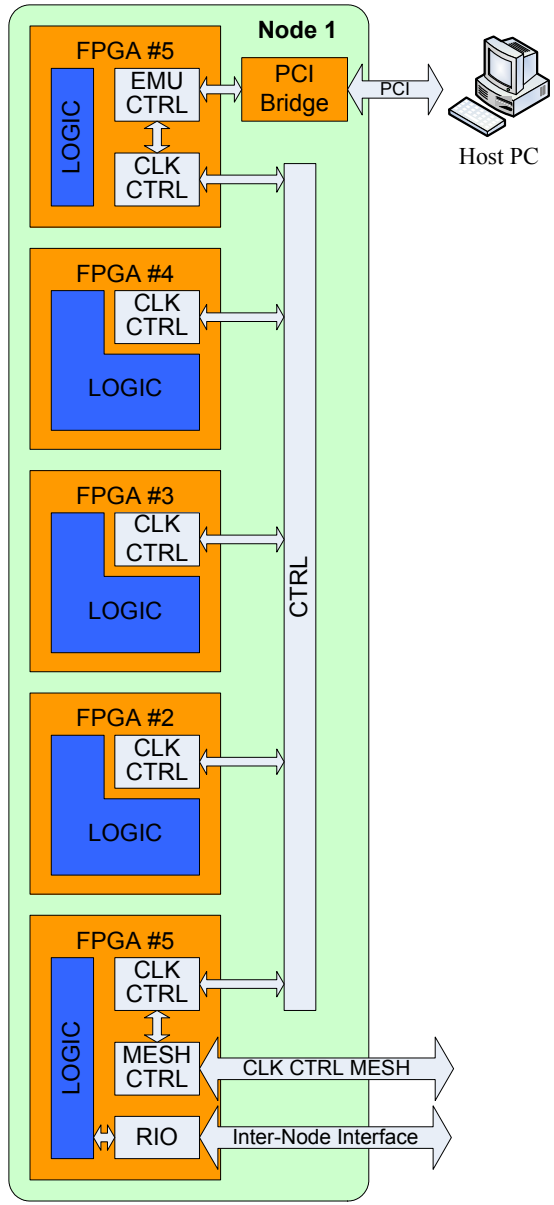
System Examples (cont.)

- Mesh architecture
- 16 RocketIO links used for 2D mesh
- 24 RocketIO links used for 3D mesh



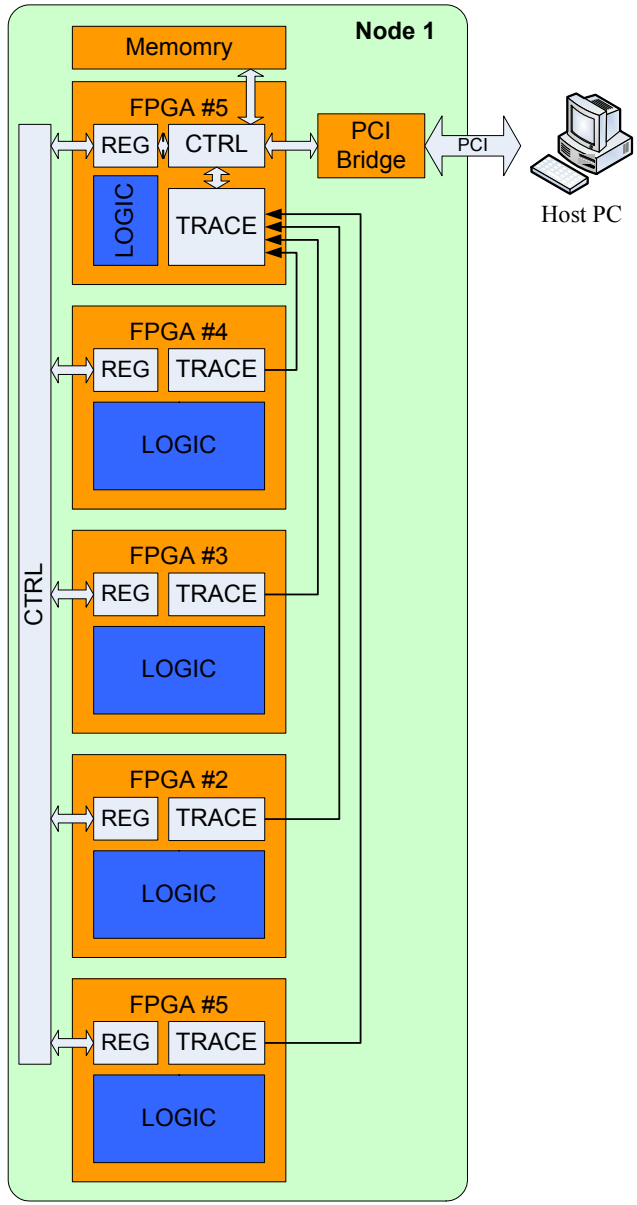
Clock Control

- Fully controllable application clock
- Application clock can be stopped via debugging software or internal logic
- Clock control used for
  - Tracing/Debugging
  - System state dump/reload
  - Data injection and reconfiguration during simulation
  - HW/SW co-simulation
- Globally synchronous system:
  - Phase corrected clock distribution across system
  - Clock control propagated across system in one application clock cycle



Tracing

- Configurable signal sample logic in every FPGA
  - Dedicated interface to central FPGA aggregating sample data
  - Application clock lowered in case of interface congestion
- On board trace memory 1GB
- Data post processed by host PC
  - Aggregation of data from multiple boards
  - Conversion to industry standard format (e.g. VCD, others)



Status

- Specification finished
- Board development of node card ongoing
- RTL development of emulation logic started
- Application RTL development started

Next Steps

- Start development of control + debug software for host PC
- RTL completion
- System bring-up