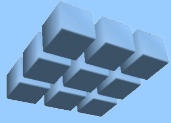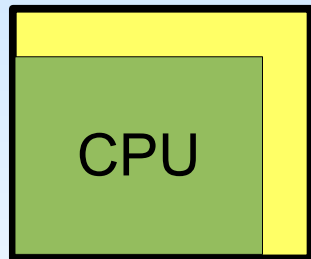# Software Development Tools for Soft Multiprocessors

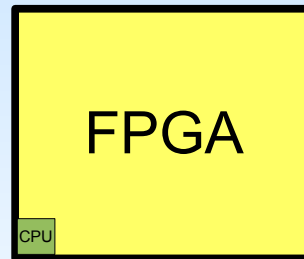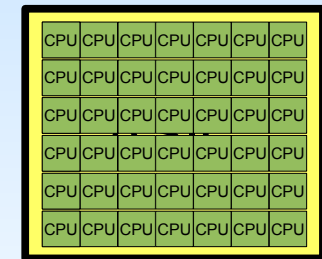## Steven A. Guccione
Cmpware, Inc.

Introduction

- One billion transistor FPGAs available (2006)

- FPGA design becoming complex

- Emerging trend: *soft multiprocessors*

  - Large, programmable IP blocks (CPUs)
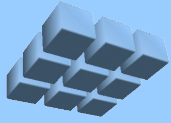
  - Hundreds of CPUs / thousands of MIPS

| CPU	FPGA CPU	CPU CPU CPU CPU CPU CPU CPU (grid)
2002 Soft CPU	**2006 Soft CPU**	**2006 Soft MP**

Processor Level Modeling

- Models (dynamically) built from:

    - **Processors**: Store and process data

    - **Memory**: Local or shared memory

    - **Links**: Transfer data between processors

    - **Networks**: A collection of links

- Simulates at the *processor* level

- Executes at up to 2M instructions / sec

- Quickly change architecture
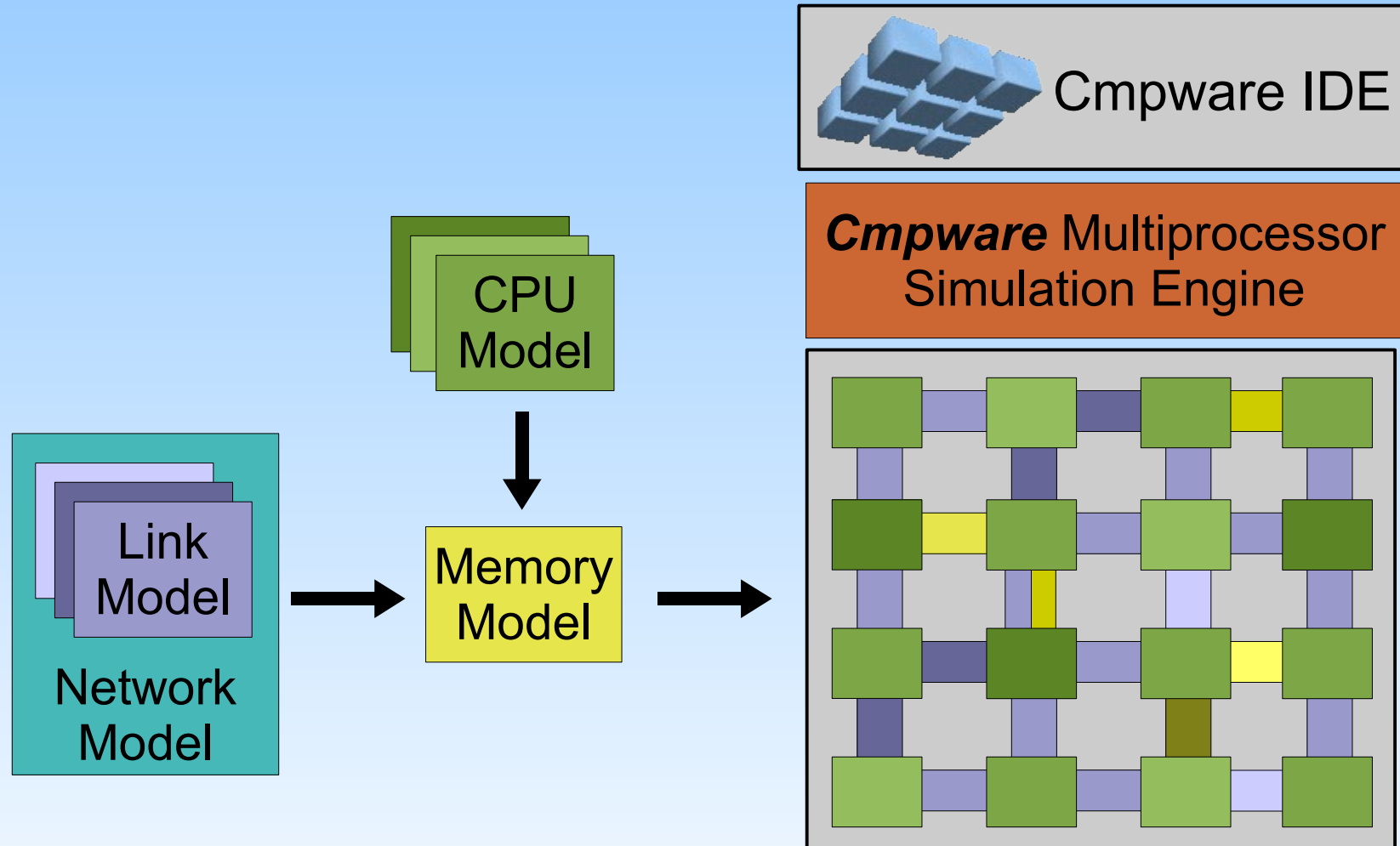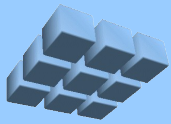
- Executes software

CPU
Model

Memory
Model

Network
Model

Link
Model
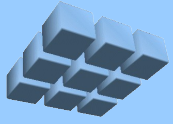
The Multiprocessor Model

The Cmpware CMP-DK
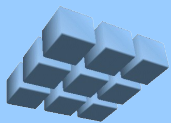
Filtering Example: Task Level Parallelism

In → **FFT** → **f()** → **IFFT** → Out
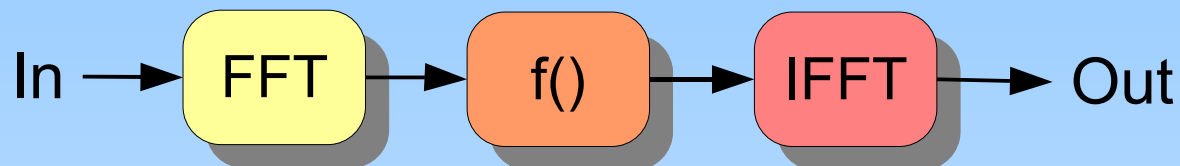
```
volatile int *x, *in, *tmp, *out;

*x = fft(*in);
*tmp = f(x);
*out = ifft(tmp);
```

in → | → **CPU** → x → | → **CPU** → tmp → | → **CPU** → out → | →

fft()　　　　　f()　　　　　ifft()
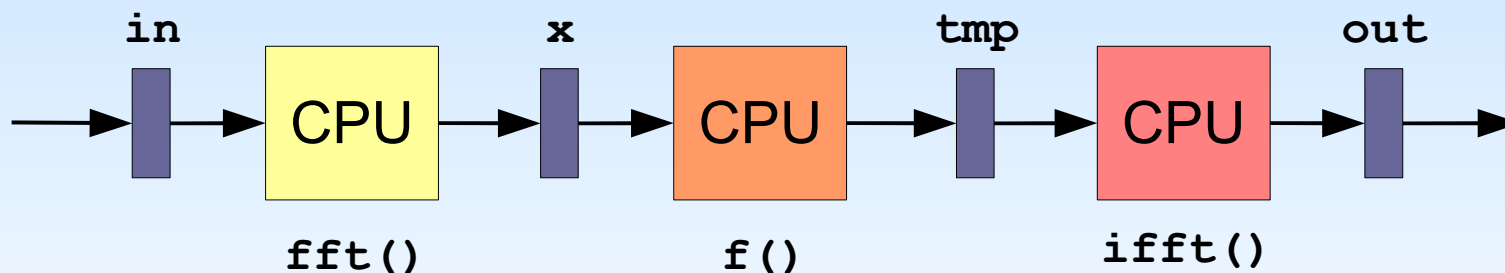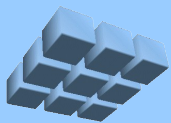
Filter Example: Sub-Task Level Parallelism
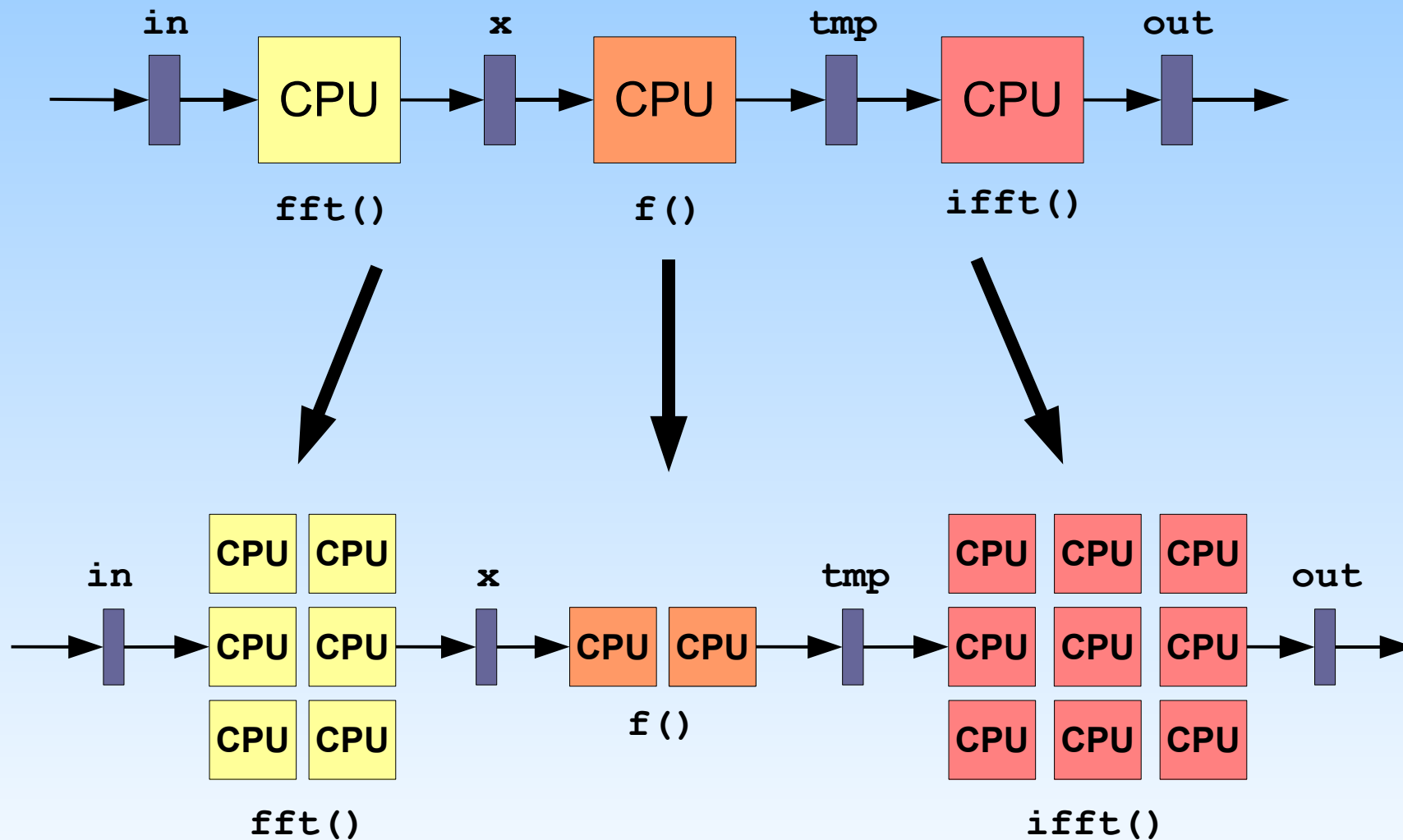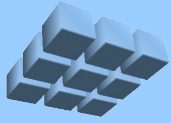
Conclusions

- Soft multiprocessing solves HW design problems (but creates SW design problems!)

- Good SW development tools essential

- Cmpware CMP-DK:

  - Quickly build and program multiprocessors

  - Redefine multiprocessor in seconds

  - Speeds simulation (2M+ instructions / second)

  - Complete Eclipse development environment

  - Standard models for NIOS, MicroBlaze, Sparc (LEON), MIPS32 and more