Investigation of Transactional Memory Using FPGAs

February 2006

Simon Grinberg
Shlomo Weiss
Mapping TM on an FPGA

- Objective: scalable TM

- Challenges:
  - DSM interconnect
  - Implementing directories
  - Support for transaction commit, abort
Implementation

- Data Memory Cluster 0
- Shared Instruction Memory
- Data Memory Cluster n
- Directory
- System switch fabric
- Local fabric
- Cluster 0
- Transaction commit/abort
- Local fabric
- Cluster n
- Transaction dispatch
Summary

- Essential FPGA features:
  - Switch fabric with variable latency
  - Softcore processors
  - Availability of development board

- Limitation: 32MB external memory