Investigation of Transactional Memory Using FPGAs

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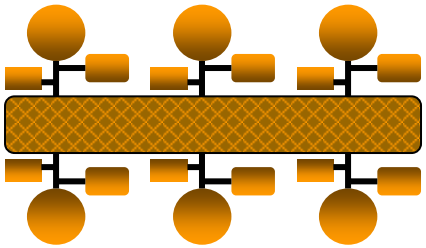
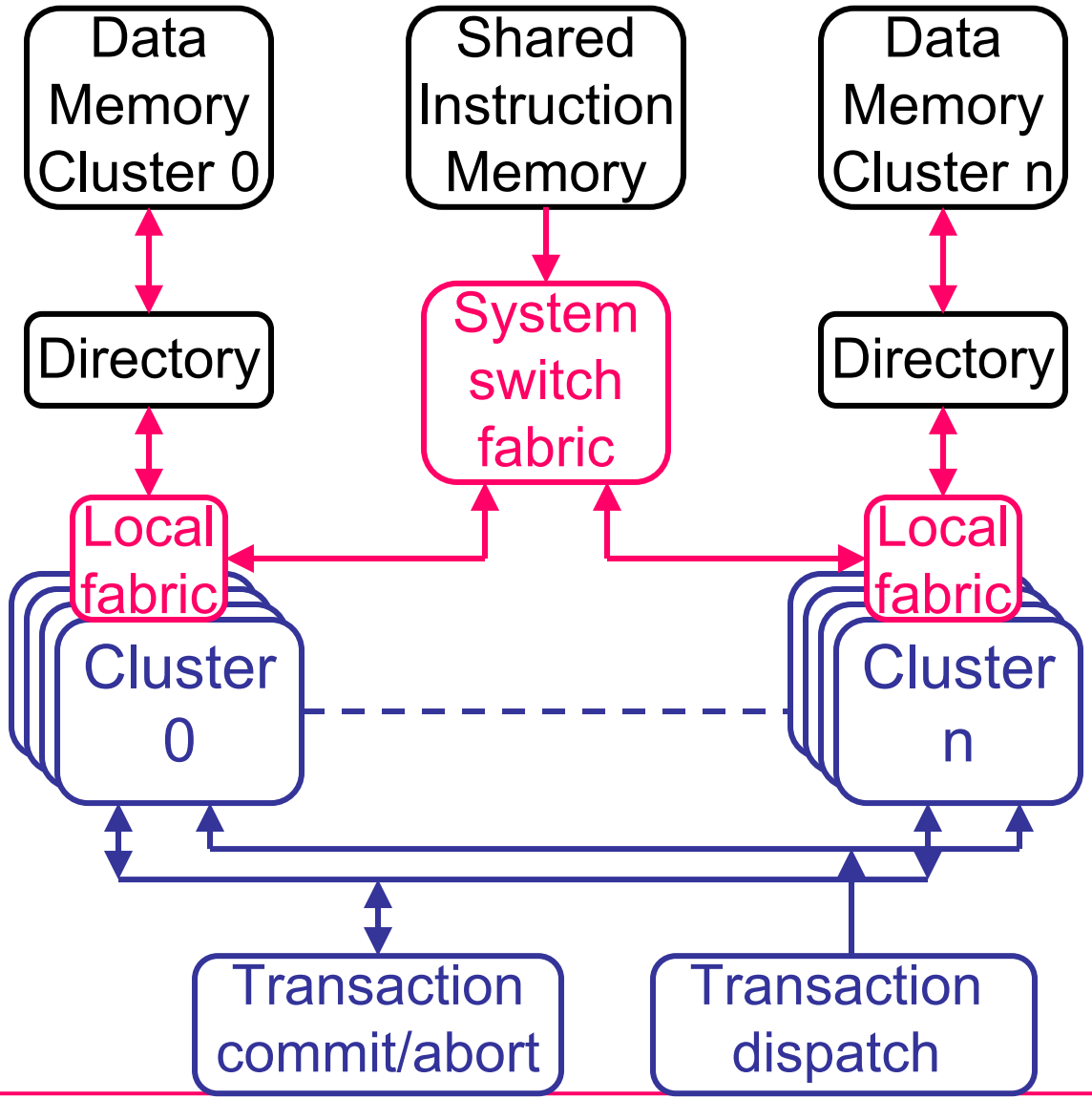
Mapping TM on an FPGA

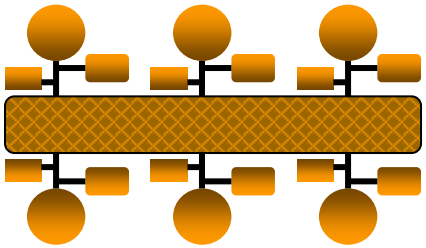


- Objective: scalable TM
- Challenges:
  - DSM interconnect
  - Implementing directories
  - Support for transaction commit, abort

Implemention



Summary



- Essential FPGA features:
  - Switch fabric with variable latency
  - Softcore processors
  - Availability of development board
- Limitation: 32MB external memory