A Scalable Processor With Embedded Software for Large-Scale Scientific Applications

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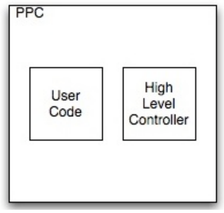
Motivation & Goals

1. Address the memory wall problem
   a) More intelligence in memory and storage usage
   b) Target the CPU, main memory, and peripherals
   c) Exploit regular scientific large-scale applications
      - For high-speed processing, reconfigurable fabric is needed
      - Use embedded RISC cores for 'slow' tasks and algorithms too difficult to directly map onto FPGA fabric.
2. RISC + FPGA fabric combination:
   a) Schedules large & fine grained data movements
   b) Associates data streams, data within streams, and mixes data streams on-chip or using latency-controlled peripherals (cache)
3. Scalability to handle large problems: Efficient Multi-Chip Configurations
4. Different mixture of processor-memory-fabric-peripheral composition

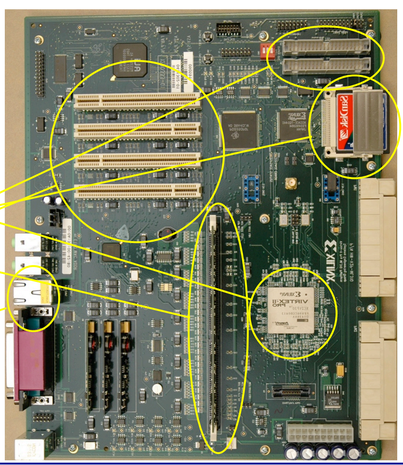
PowerPC: A High Level Controller

•PowerPC (PPC) core (with some hardware additions) can execute user programs
•PPC core may also perform control and monitoring functions for the processor system

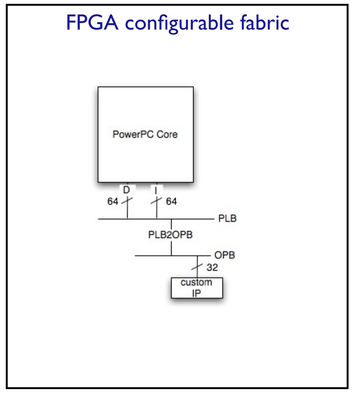


ML310 Development Board

- XC2VP30 FPGA with 2 PowerPC 405 RISC Cores
- 256 MB DDR DRAM
- SanDisk
- IDE interfaces
- PCI
- Ethernet



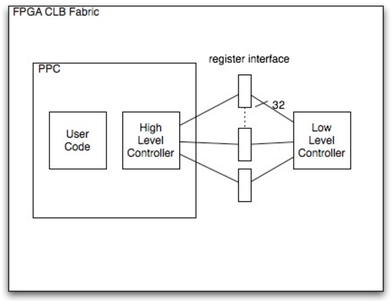
PowerPC - Custom IP Interface



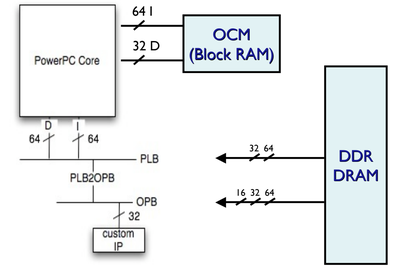
High Level Controller Features

1. Peripheral latency monitoring
   - Store delays between data request and data arrival for each peripheral
2. Peripheral data prefetch control
   - Begin retrieving data streams and process immediately or buffer locally, based on latency values
3. Peripheral resource scheduling
   - Control access to peripherals
4. Coarse-grained data association, mixing, and buffering
   - Vectorized data streams allow the controller to associate streams with each other (dependencies), re-order data into memory buffers (useful in matrix-matrix multiplication and transposes), etc.

HLC - LLC Interaction



PowerPC - Custom IP Interface Memory Options



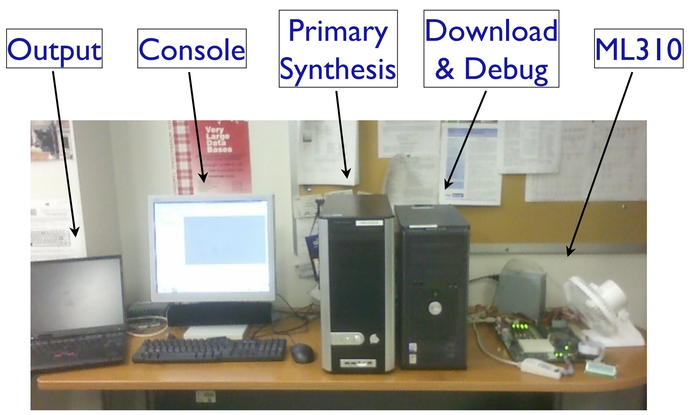
Low Level Controller Features

1. The LLC is the Custom IP shown above, connected to the OPB
   - LLC is unique for each application.
2. The LLC resides within the FPGA's configurable logic blocks (CLBs)
   - Reusable functional logic can be dynamically mapped onto CLBs at compile-time or run-time.
3. The LLC performs both computations on the data streams and fine-grained data mixing
   - Control signals exchanged with HLC to indicate status of buffers, dout_rdy, etc.
   - Data element arithmetic operations (int/FP) performed at this level. Elements in streams may be remixed to satisfy output constraints, dependent instructions, etc.

Conclusions

•Fast peripherals need not be limited by intermediate controllers, buses, and operating systems.
•Controller logic can be integrated alongside traditional processor components in a single package.
•Intelligent use of memory peripherals on local buses reduces processing latencies.
•Embedded software saves resources better devoted to time-sensitive computation.

Experimental Setup



More information including additional slides and related work is available at http://pages.poly.edu/~dfinke01 or by email to dfinke01@cis.poly.edu