# Design Tool for Rapid System Prototyping on FPGAs

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CPU architects who evaluate their systems on FPGAs need to balance the time and effort spent on the CPU architecture with the time and effort spent creating the systems that they evaluate. The flexibility of FPGAs lets a researcher test one or more CPUs in a variety of systems on the same hardware, but each system must be designed and debugged. Tools that automate the system-creation process help increase the variety and quantity of test systems.

The system-design tool SOPC Builder converts a system-description file into VHDL or Verilog files that can be synthesized into an FPGA configuration. The tool also generates corresponding C/C++ header files that describe the memory maps seen by all of the master ports in the system. In addition to conversion facilities, SOPC Builder provides a graphical system-description-file editor.

Areas of design automation provided by SOPC Builder include the generation of address decoders, data-path multiplexers, slave-side arbiters, dynamic bus resizers, wait-state generators, interrupt controllers, and metastability-hardened clock-domain crossers. The tool supports variable-latency transactions, streaming transactions, and burst transactions.

CPUs described using VHDL or Verilog can be imported as system components. One or several instances of these components can be instantiated into systems along with on-chip memories, off-chip-memory interfaces, PIO interfaces, and other embedded-system components and interfaces.

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