Design Considerations for FPGA-Based High-Performance CPUs

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CPU designers who target FPGAs face different tradeoffs than designers who target ASICs. Unaware of FPGA tradeoffs, an ASIC designer may see an unexpected imbalance in timing paths leading to a slower design. Even when FPGA performance is not a requirement (as in prototyping), some ASIC circuit blocks will map inefficiently into FPGA resources. A designer who knows relative FPGA resource costs and speeds can create a more efficient CPU. For example, a general-purpose embedded CPU has been designed that performs 150 Dhrystone MIPS on a 130-nm FPGA and uses only 1,200 logic elements.

ASIC designers will see that adders in FPGAs are fast, cheap, and plentiful. Registers in FPGAs also are fast and cheap, although it is best when they are driven by at least a small amount of combinatorial logic. In some FPGAs, multipliers are fast. Memories in an FPGA are dual-ported, and so designers should take advantage of the second, essentially free, port whenever possible. Leaving the second memory port unused does not save resources or improve performance because FPGA RAM cells remain dual-ported regardless of port usage.

ASIC designers will see that wires and multiplexers are slower and that adding just one more input to a multiplexer may slow performance unexpectedly. Wide equality comparators, such as those used for tag comparisons, are slower and so must be used carefully. On-chip RAMs, although feature-rich, will be slower than RAMs on ASICs. Full barrel shifters on FPGAs will require more than a single clock cycle or stage to complete their operation.

On-chip RAMs with more than two ports will be limited to a single write port unless the write port is time-multiplexed or the remaining ports are in a read/write configuration.

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