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Toward A Common Emulation Infrastructure with Large-Scale FPGA

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1 Introduction

The diversification of processor architectures and applications result in long simulation time when using detailed software simulators. The measured simulation time of sim-cache in SimpleScalar toolset[1] is summarized in Table 1. The sim-cache is a cache simulator implemented on a fast functional simulator. The data is obtained on a computer with PentiumIII Xeon 700MHz, 512 main memory. It is shown that the simulation time per program requires a long time of 4 hours or more.

Table 1: Simulation speed of sim-cache.

Program	inst	Time	inst/sec
099.go	35 billion	5.3 hour	1.88 million
129.compress	43 billion	6.5 hour	1.82 million
134.perl	24 billion	4.0 hour	1.66 million

The major research goal of our project is to build a common hardware platform to emulate various processor architectures. We are developing a hardware emulation infrastructure with large-scale FPGA and our first target is a fast and flexible cache system emulation.

2 Hardware emulation with FPGA

A process to design new processor architectures is shown in figure 1. Functional simulators are used in the early phase of the design process. Then detailed performance simulators are used. Our hardware emulation tries to shorten the simulation time of the first phase, the shaded part in figure 1.

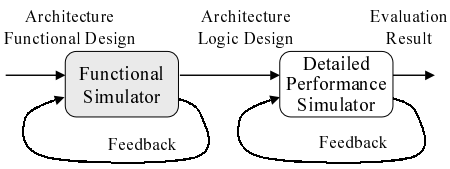

Figure 1: Flow in a microprocessor design process.

The block diagram of our hardware emulation is shown in figure 2. Large scale FPGA, two DRAM and four SSRAM is the main component. A processor, memory controller logic and a target cache system are implemented in FPGA. SSRAM and DRAMs are used as a part of L1, L2 cache and the main memory.

Our target clock speed of the system is 40MHz. If a processor on FPGA achieves IPC(instructions per second) of 1 with the pipelining, the total throughput of the hardware emulation achieves 40 MIPS(million instructions per second). This is 20 times faster than a software simulator sim-cache of about 2 MIPS.

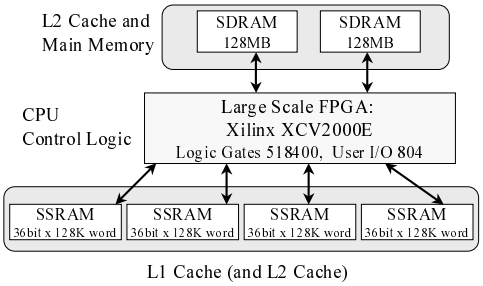

Figure 2: Block diagram of a hardware emulator.

3 Present status and future plan

We are developing an Alpha processor core and cache systems on a FPGA board. This version of processor core has no floating-point register and unit. It is written in Verilog-HLD and synthesized with Xilinx Foundation ISE. The floor plan of the processor core is shown in figure 3.

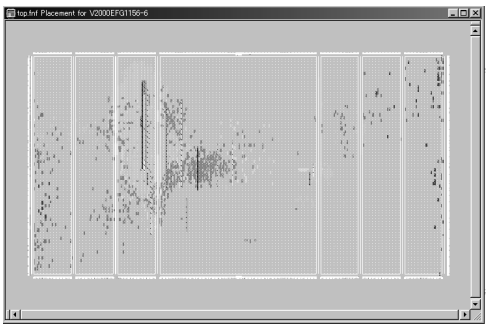

Figure 3: A placement result for V2000EFG1156.

Our target FPGA is Xilinx V2000E. Even if a 64-bit processor core is implemented, it occupies only 12% of the hardware resources. We confirmed that the clock speed of current implementation is 30MHz.

Our future plan includes an efficient implementation of system calls in order to run SPEC CPU benchmark.

References

[1] Doug Burger and Todd M. Austin. The SimpleScalar Tool Set, Version 2.0. Technical report, University of Wisconsin-Madison, 1997.