**A Flexible Architecture for Simulation and Testing (FAST) Multiprocessor Systems**

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The Flexible Architecture for Simulation and Testing (FAST) uses simple processors combined with state-of-the-art FPGAs and memory chips on a single board to create a flexible simulation fabric that can execute millions of instructions per second. FAST is a unique chip prototyping substrate because it provides the flexibility of software simulation with speeds at least 3 orders of magnitude faster and an order of magnitude faster than hardware emulation with a generic array of FPGAs. FAST provides a flexible chip performance evaluation substrate for detailed investigation of topics including multiprocessor and chip multiprocessor (CMP) design, memory system design, thread-level parallelism (TLP) extraction techniques, ISA extensions, parallel software design with both low-level operating systems and applications, and reconfigurable architectures.

FAST is composed of four processor tiles. As shown in Figure 1, each processor tile contains two Xilinx XCV1000 FPGAs, a MIPS R3000 CPU, a MIPS R3010 FPU, and 256K x 36 bits of dual ported processor-local SRAM. An integral component of the processor tiles is the flexibility provided by the two FPGAs. One FPGA functions as the processor-local memory controller while the other adds new coprocessor functionality, if desired. The MIPS CPU and FPU chips are being used in combination with the FPGAs for several reasons. First, they provide an exposed L1 memory and coprocessor interface. The presence of the FPU expands the application domain to include applications heavily dependent upon floating-point instructions that would be impractical to run with slow floating-point emulation. Second, using a simple hard processor core leverages its highly optimized datapath, which is better suited for word-size data manipulation than FPGA logic blocks.

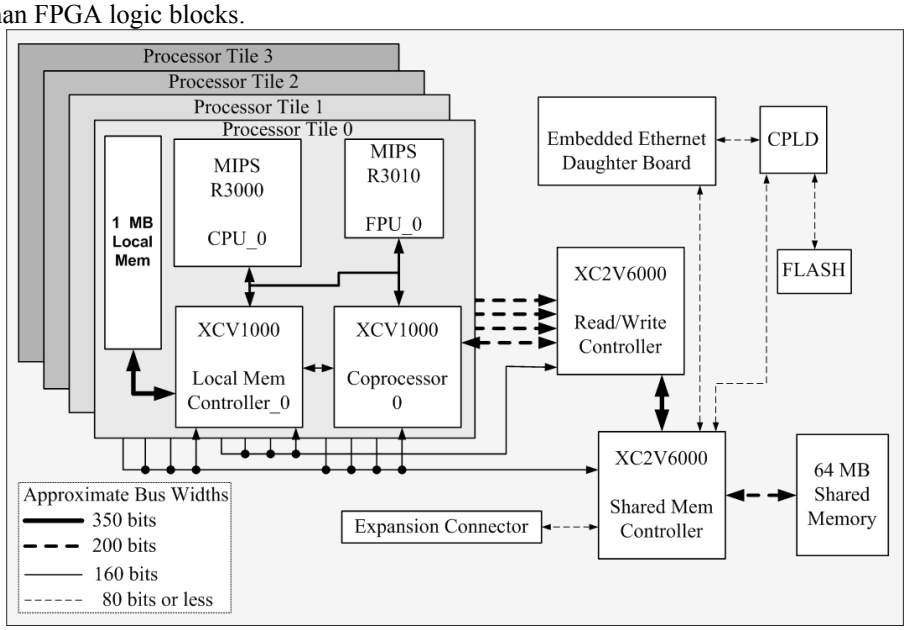


**Figure 1.** FAST high-level component diagram with major buses.

Two Xilinx XC2V6000 FPGAs connect the processor tiles together and manage the shared memory banks, the TCP/IP Ethernet interface and the expansion interface. The first FPGA is used as the shared-memory controller, managing 16M x 36 bits of SRAM. This FPGA also controls an expansion connector that can be used for arbitrary digital interfaces, including communication between multiple FAST PCBs. The second Xilinx XC2V6000 acts as the central hub of the design, connecting the processor tiles and the shared-memory controller using wide buses and providing a large amount of logic to manage any interactions. A Xilinx CPLD provides the glue logic necessary to program the FPGAs, monitor the state of the board, interface to the board configuration memory, and other auxiliary functions. A daughter card with an embedded microcontroller and Ethernet port provides the external communication interface.

The FAST prototyping substrate will enable a more thorough investigation of architectures that employ fine-grained threading, speculative threading, and chip multiprocessing. We initially intend to exploit FAST's prototyping potential by using the Hydra CMP design to explore TLS and other multithreaded architecture topics. Unlike software simulators, FAST will be able to provide detailed execution statistics without any degradation in performance, because complete architectural evaluation of the memory and processor subsystems can be performed using statistic counters embedded in the FPGAs. FAST has full control over the various system latencies relative to the fixed processor cores, enabling on-chip and off-chip memory system design exploration and making FAST a rapid prototyping substrate for a variety of static and reconfigurable systems.