Experiences with Multiprocessors Designs in Multiple FPGAs

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Abstract

At White Eagle we have developed a system and mapping techniques that have shown to be very useful in implementing hardware prototypes of multiple processor SoCs. In applying these techniques to several actual designs we have discovered several useful application theorems that yield astounding results. The 15 minute presentation will be conducted by the William Wu, the Principle Investigator. He will address the following points.

1. summarize the theoretical basis for minimizing the number of interconnections between FPGAs in systems requiring multiple FPGAs
2. present the results of three SoC designs containing multiple processors or application specific computation units
3. present the issues and solutions to handling analog and digital I/O's
4. talk about the problems with interfacing to memories including DDR memories
5. summarize the concerns and increased productivity of the embedded software developers
6. discuss the application of formal verification of the SoC RTL versus FPGA implementation

Figure 1 illustrates the typical hardware setup. The FPGA board and analog I/O boards are interfaced to the two workstations; one is for programming and controlling the FPGA and the other is for software development. Additionally the SoC prototype is emulating the chip and is connected to the system development board for full system integration testing.

After presenting the important points of interest, the Author will actively participate in the discussion and can specifically address the following points

* Case studies from use in SoC development
* Platforms: design of hardware to support architectural exploration
* Multiprocessor designs on one FPGA or across multiple FPGAs
* Handling I/O
* System software support for FPGA prototypes
* Instrumentation: gathering dynamic statistics
* Validation: checking correctness

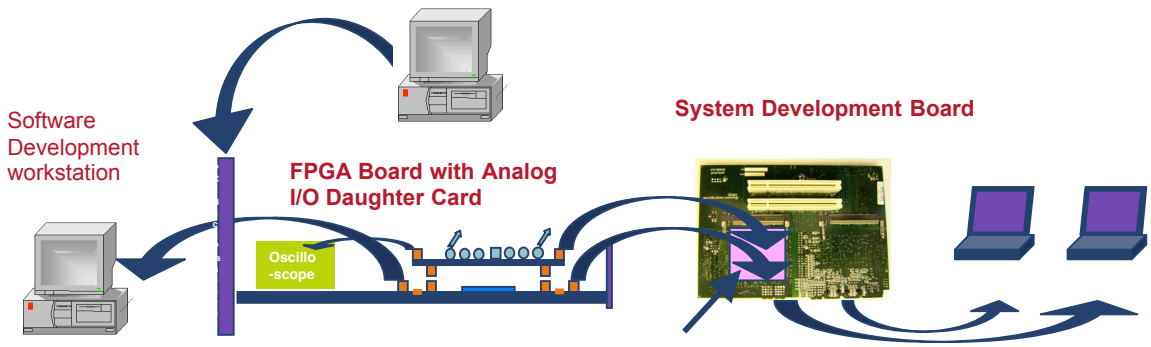

Figure 1 – Typical System Setup