

FPGA-based Emulation Platforms at the Berkeley Wireless Research Center

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We have several projects at the Berkeley Wireless Research Center (BWRC) related to using FPGAs for architecture emulation and custom IC development. The first system we built for this purpose was the Berkeley Emulation Engine. It was constructed in 2002 and comprised 20 Xilinx V200E FPGAs. Since then it has been in near constant use aiding in the design and verification of a variety of communication and sensor processing architectures and IC implementations.

The most ambitious prototyping project to date is a collaboration between BWRC and Infineon on the design of a low-power processor and SOC targetting software defined radio. The key feature in this SOC is a multi-core SIMD cluster capable of performing digital baseband processing of many different wireless protocols. Work at BWRC includes design and emulation of the SIMD cluster using the BEE system. A Simulink/System-Generator environment is used for the design of the SIMD core, and the Xilinx EDK is used to generate a Microblaze processor core as the control processor to the SIMD cluster. A variety of architectural and emulation issues are being explored, including investigating the optimal number of contexts per SIMD core, using multiple microblaze cores to simulate a multithreaded processor, and mapping shared memory to the external SRAM on the BEE.

We are also currently in the middle of the development of the second generation hardware platform and its associated programming tools. The BEE2 system is based on Xilinx Virtex 2VP70/100 and is scalable from 5 to 100s of FPGAs. We are developing new tools that enable incremental design development and interactive debugging and verification.

At the workshop, we propose to describe our FPGA-based emulation platforms and tools and our experience using these systems for developing new chip architectures.