

New Opportunities for Computer Architecture Research Using High-Density FPGAs and Design Tools

Patrick Akl, Nahi Abdul-Ghani, Mohamad El-Majzoub, Maroulla Haddad,
Siba Harb, Marwan Simaan, and Mazen A. R. Saghir
Department of Electrical and Computer Engineering
American University of Beirut

{pea02, nha15, mte01, mgh09, shh15, mjs05, mazen}@aub.edu.lb

Abstract

The proliferation of high-density FPGAs and powerful design tools have paved the way for new applications for these versatile chips. In addition to the availability of millions of logic gate equivalents, rich on-chip features like multipliers, memory blocks, and hard CPU cores have transformed FPGAs into powerful computational platforms. These, in turn, are paving the way for new directions in computer architecture research and providing fresh opportunities to evaluate new architectural ideas under realistic implementation constraints.

In this presentation, we report on our experiences with two, on-going, research projects at the American University of Beirut. Both projects rely on the availability of high-density FPGAs like the Xilinx Virtex-II, and design tools like the Xilinx EDK and ISE, to study the design trade-offs involved in extending the functionality of a soft CPU core and the effectiveness of a new design tool for implementing application-specific instruction processors (ASIPs) in FPGAs, respectively.

Our first project involves designing and implementing an IEEE-754 compliant floating-point unit (FPU) for the Xilinx MicroBlaze soft CPU core. The goal of the project is to assess the impact of different organizational models on instruction-set architecture, execution performance, and area. In the first model, the FPU is a co-processor that is connected to the CPU core through high-speed communication channels called Fast Simplex Links (FSLs). In the second model, the instruction-set architecture and datapath implementation of an open source version of the CPU core are modified to support new floating-point instructions and an integrated floating-point unit, respectively. Both models are compared to the baseline MicroBlaze CPU, which uses a library of software routines to support floating-point operations.

Our second project involves developing a design tool for synthesizing the datapath of a VLIW-based application-specific instruction processor (ASIP). This tool is part of an automatic ASIP design environment called *Arabesque*, and it allows us to explore an architectural design space using actual data on execution performance and area. Our tool reads a number of architectural parameters from a configuration file, including data word length, number and type of functional units, size of register files, and availability of custom instructions, and generates behavioral and structural VHDL code for the corresponding datapath. The VHDL code is then synthesized and mapped onto a Virtex-II FPGA using the Xilinx ISE tools. The performance and area of various synthesized datapaths are then examined to assess the effectiveness of our design tool.