FPGAs for Temperature-Aware Microarchitecture Research

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Motivation

- Temperature fast becoming a constraint to increasing performance
- HotSpot [ISCA 03] – tool that can be integrated with power performance simulators to predict temperature
- Use FPGAs to analyze
  - micro-architecture/temperature interactions
  - validate HotSpot

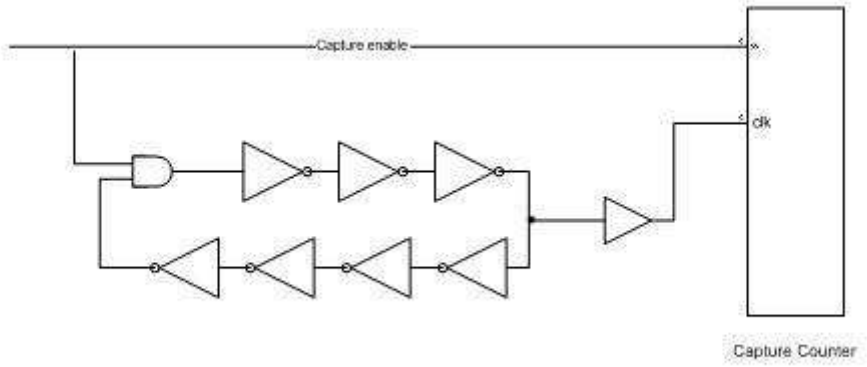
Methodology

- Implement temperature sensors on the FPGA fabric
- Instantiate sensors at various locations on the FPGA along with a soft-microprocessor under test
- A simple controller can read the temperature from the sensors and control the activity of the system.

Experimental Setup

- Ring oscillator based temperature sensor
- Xilinx EDK/ISE software
- Xilinx XC2VP7 device on an Insight Memec board
  - Embedded PowerPC used as the controller
  - MicroBlaze used as the processor under test
- FPGA core powered using constant DC supply that allows measurement of current

Temperature Sensor Schematic

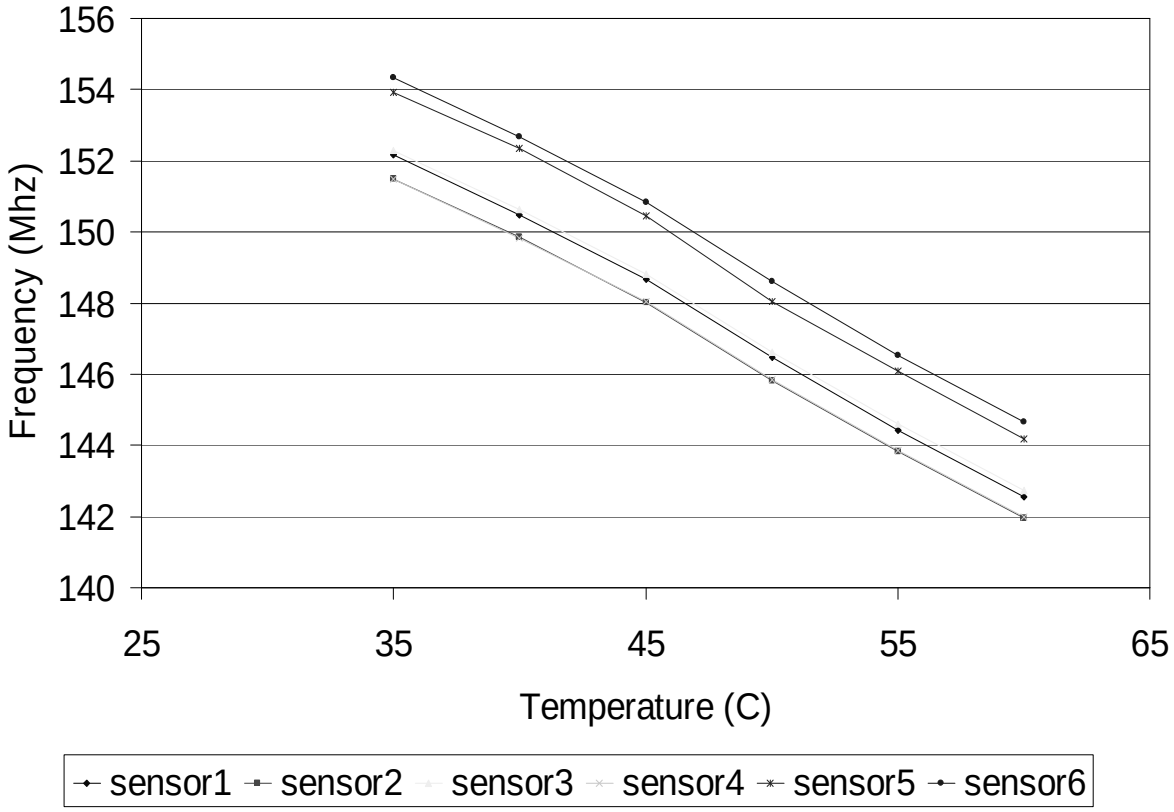


Sergio Lopez-Buedo and Eduardo Boemo,
Making Visible the Thermal Behavior of Embedded Microprocessors on FPGAs, FPGA 2004.

Sensor Implementation

- Each NOT can be implemented in a single LUT.
- Each of the LUTs have to be manually placed (RLOC constraints)
- To achieve similar frequencies, the LUTs need to be manually routed as well.

Sensor Calibration



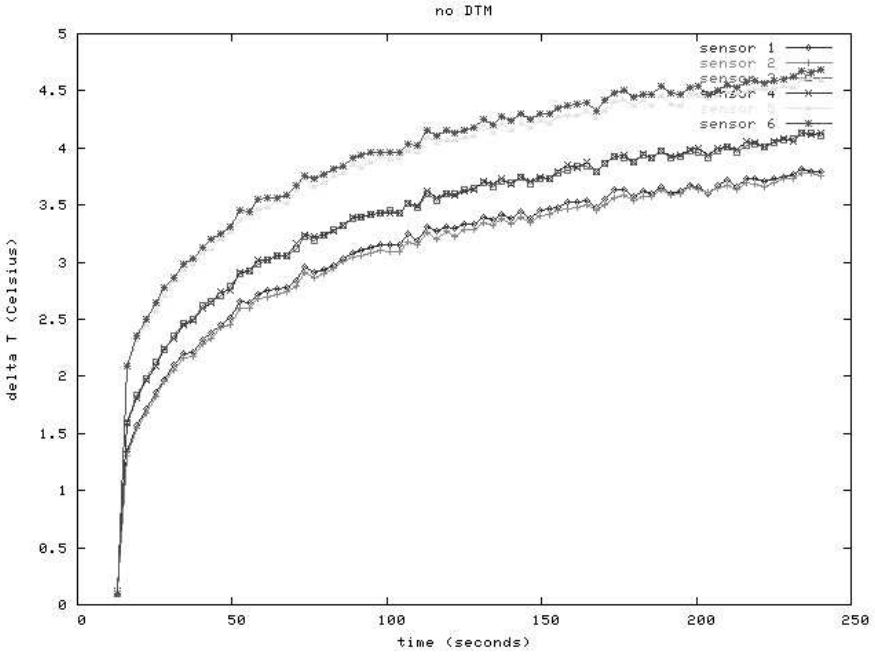
Application 1: Granularity of Temperature Variations

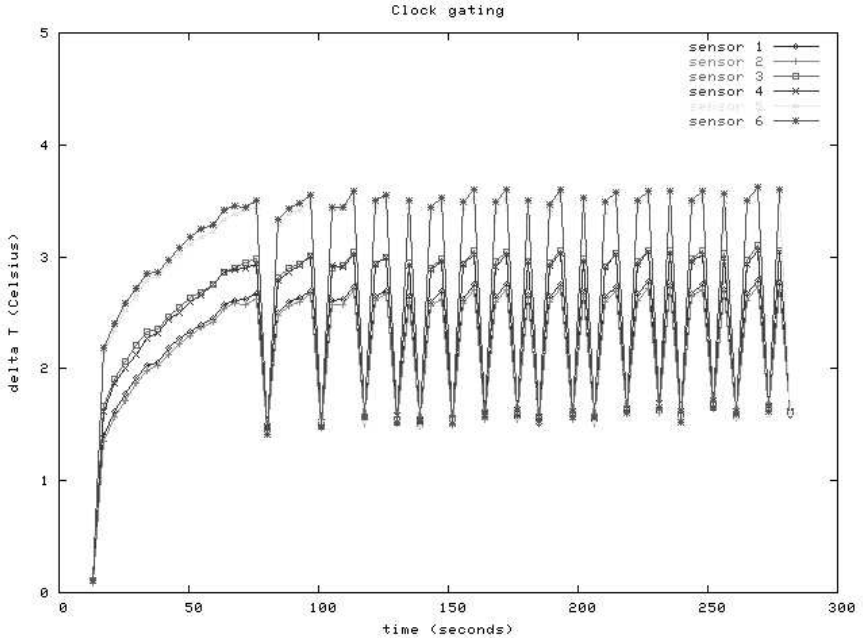
- Attempt to determine how big an area is needed to create a local HotSpot
- Method:
  - Create a “heater” unit
  - Sorround it by sensors
  - Vary the size of the heater unit and vary the distance between different heater units.

Application 1: Granularity of Temperature Variations

Heater size	Distance bet. Heater units		
	Close	Medium	Distant
2 slices	2.81	2.71	2.66
4 slices	4.15	3.40	3.06
8 slices	6.86	6.82	6.62

Application 2: Clock gating





Application 3: Comparison with HotSpot

Unit	Power (mW)	Sensor	HotSpot
blank1	0.1	3.4	3.37
left_ppc	75	3.5	3.69
bot_ppc	75	3.4	3.67
ppc	45	3.5	3.66
mb	313	4.1	3.96
blank2	0.1	3.4	3.38

Challenges

- Dependence on Vdd
- Vdd bounce/load
  - Especially when coupled with clock gating
- “Simple” soft-processors
- Core implementation differs from custom microprocessors
  - Area
  - frequency
- Power models

Conclusion

- Testbed for temperature-aware micro-architecture experiments.
- Easy to implement, fine grained granularity
- Validated HotSpot steady state temperatures to within 10%.