Evaluation of Memory Sub-sytem Performance with FPGAs

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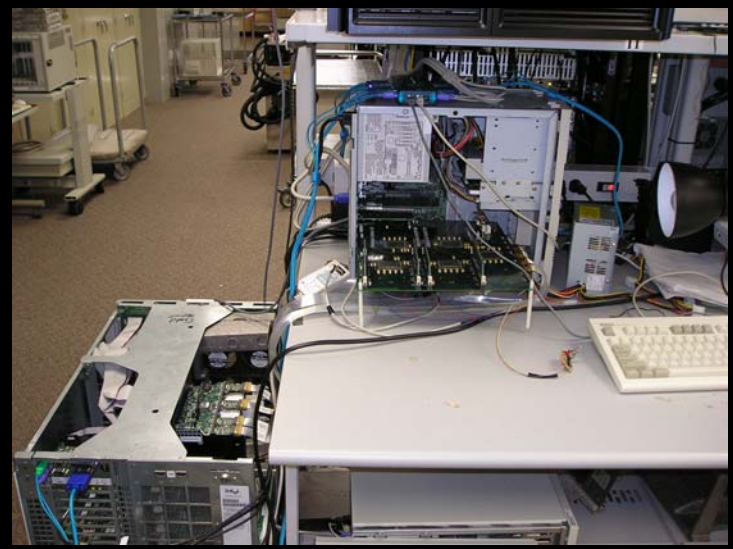
Recent and Current Projects

- PHA$E – Programmable Hardware Assisted Cache Emulator
- ACE – Active Cache Emulator
- PMI – Programmable Memory Interface

Programmable Hardware Assisted Cache Simulator (PHA$E)

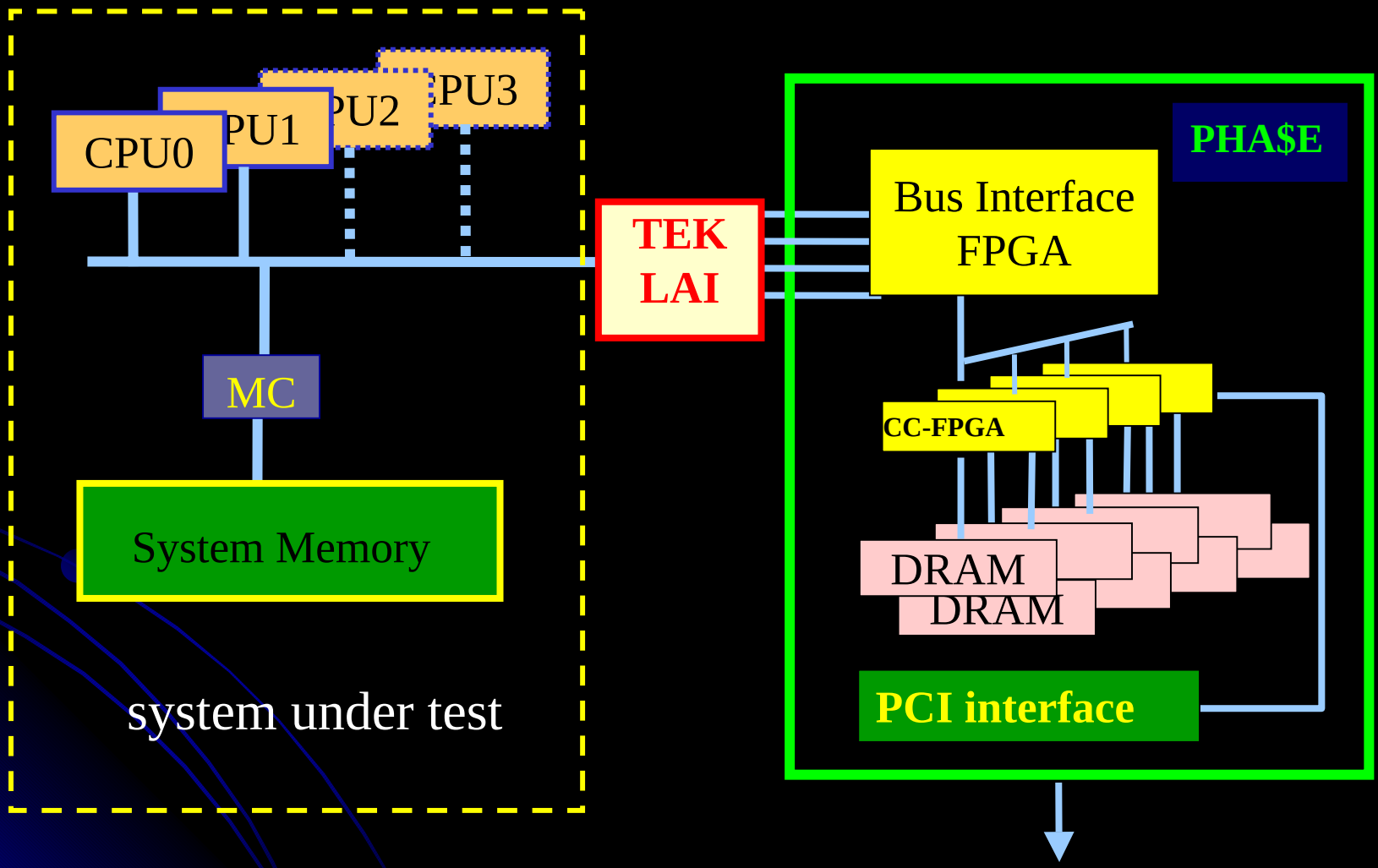
- Real-time FPGA based cache simulator.
- Collected cache organization studies for several server workloads on PIII.
- Results published (FPL'03, WWC'03, CEACW'04)

2P

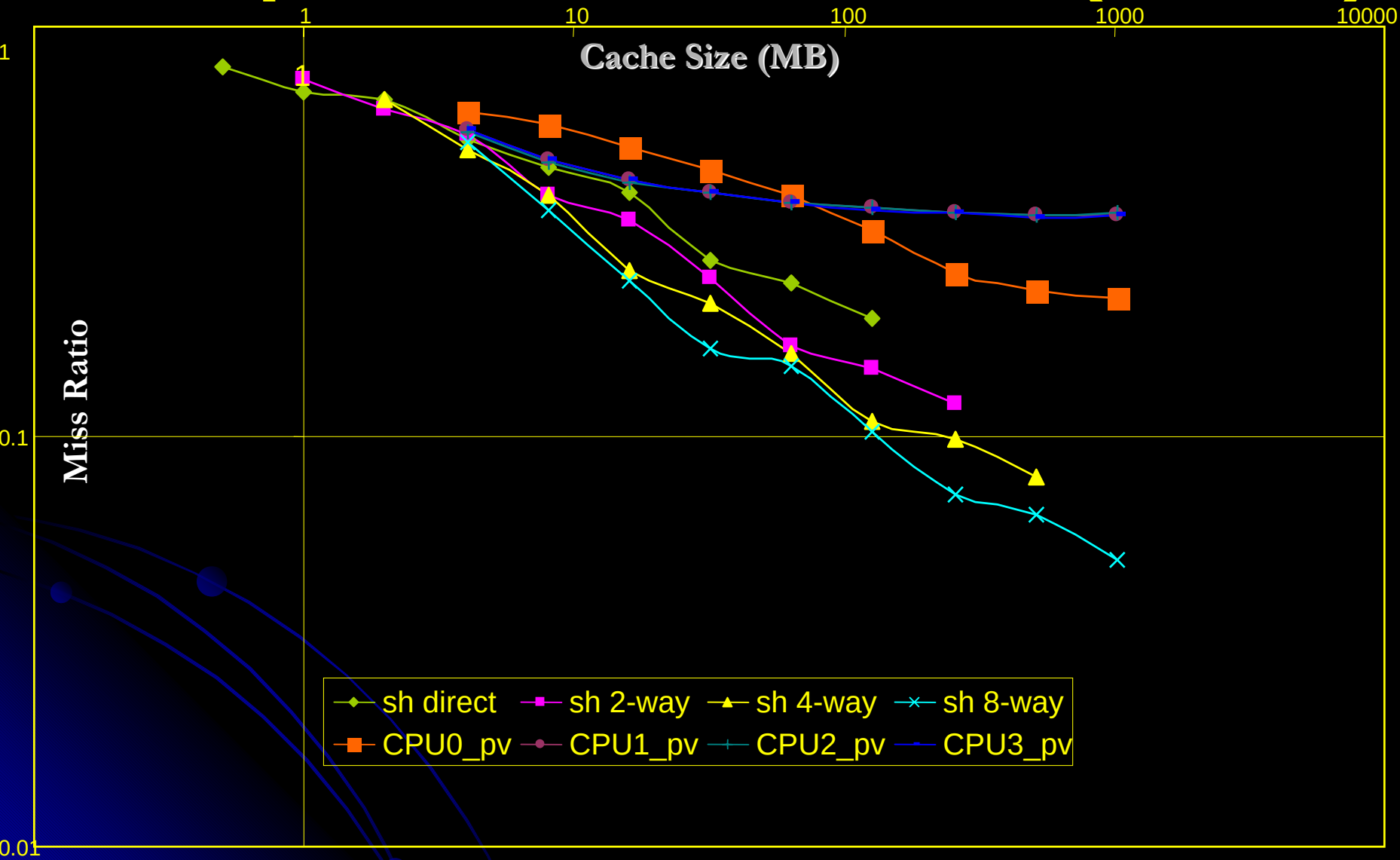


4P

System Block Diagram

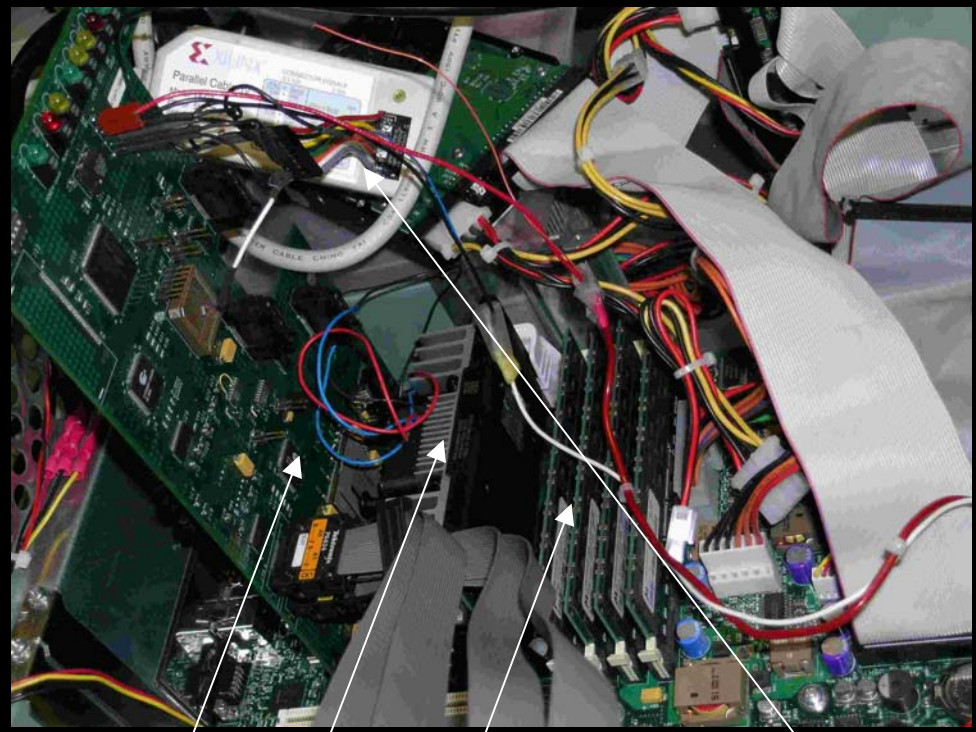


Sample PHA$E Results (TPCC)

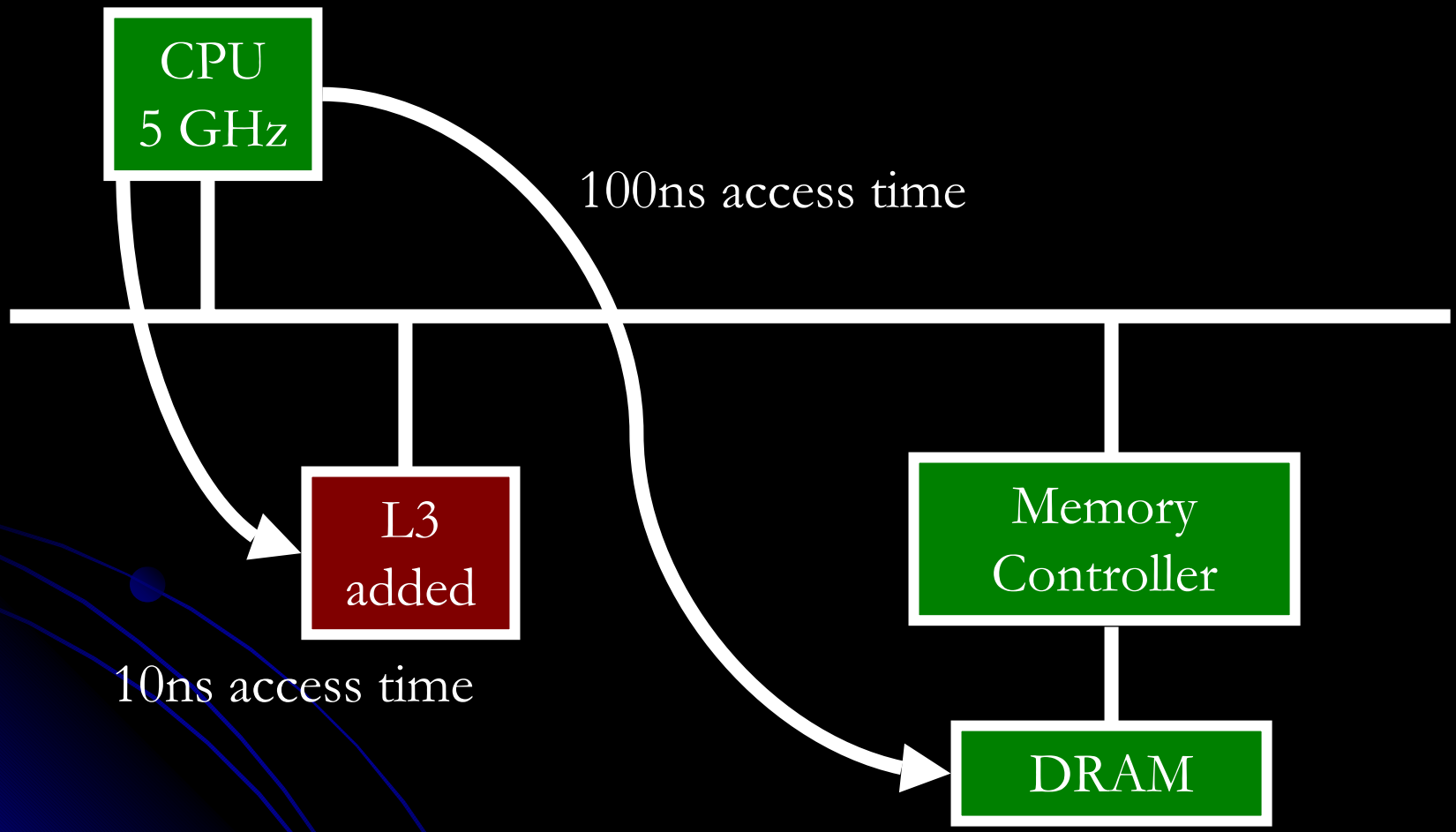


Active Cache Emulator (ACE)

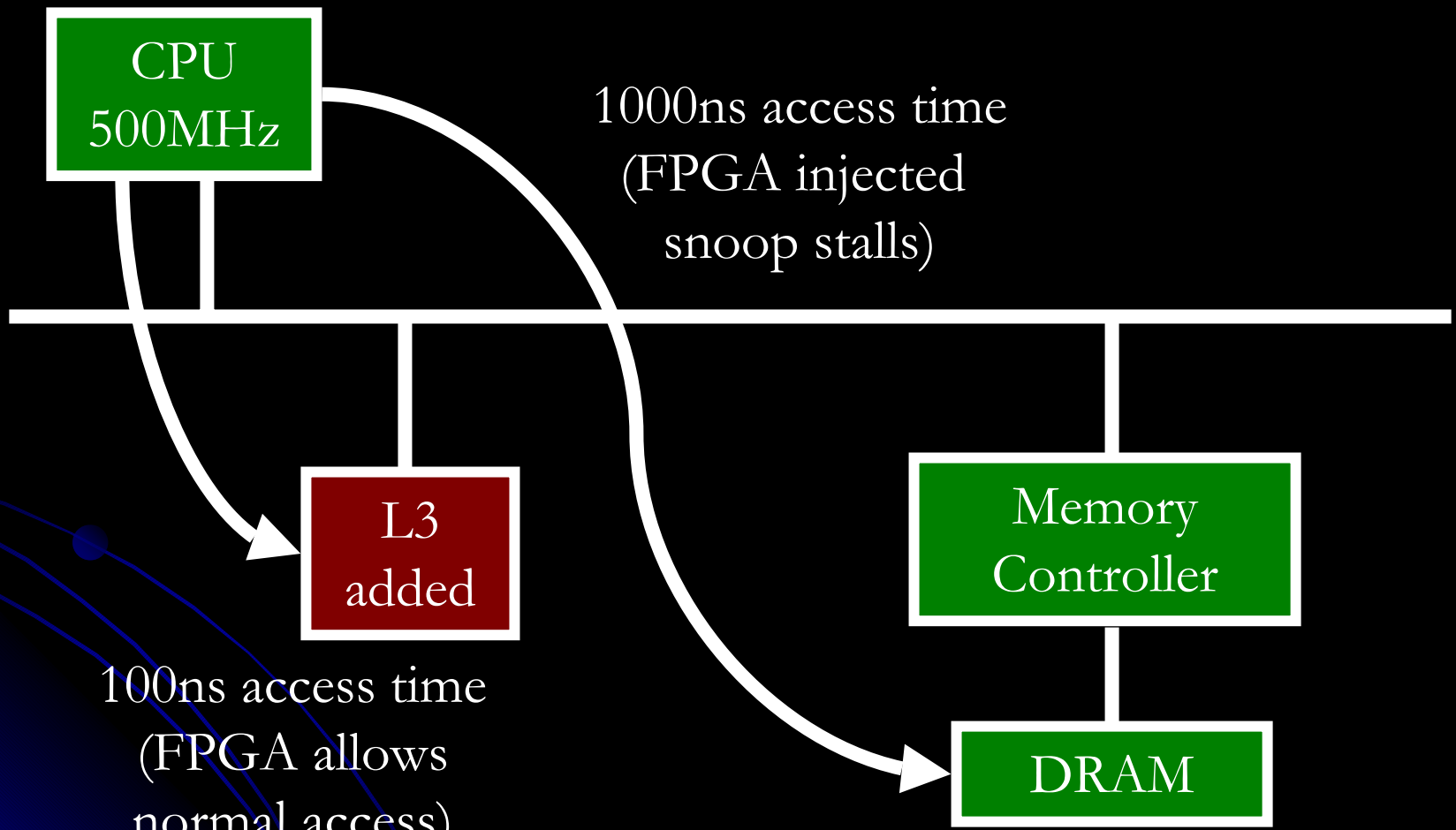
- Active emulation on processor bus
- System with variable time dilation
- Provide performance analysis and miss ratios



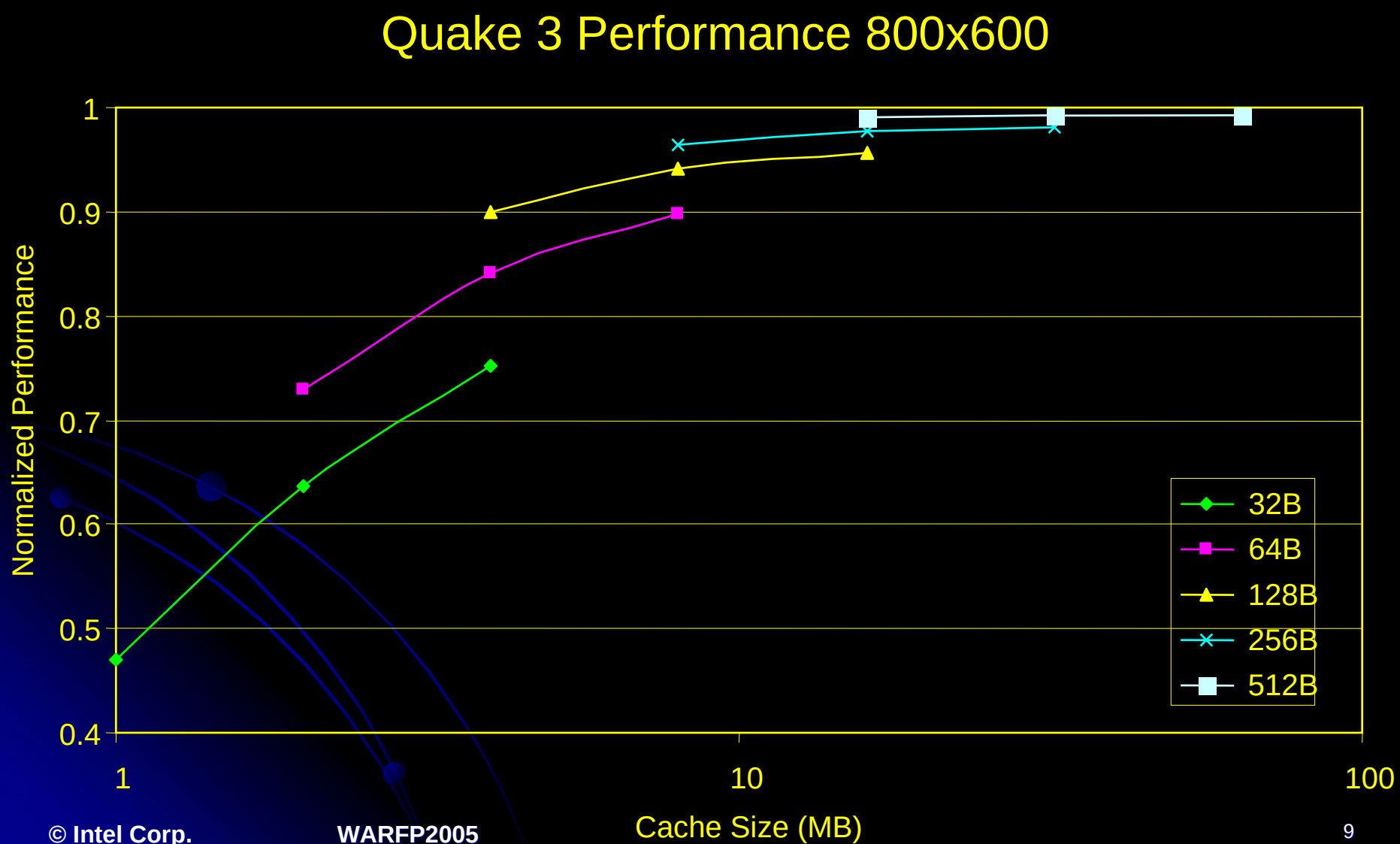
ACE Block Diagram



ACE Time Dilation Example

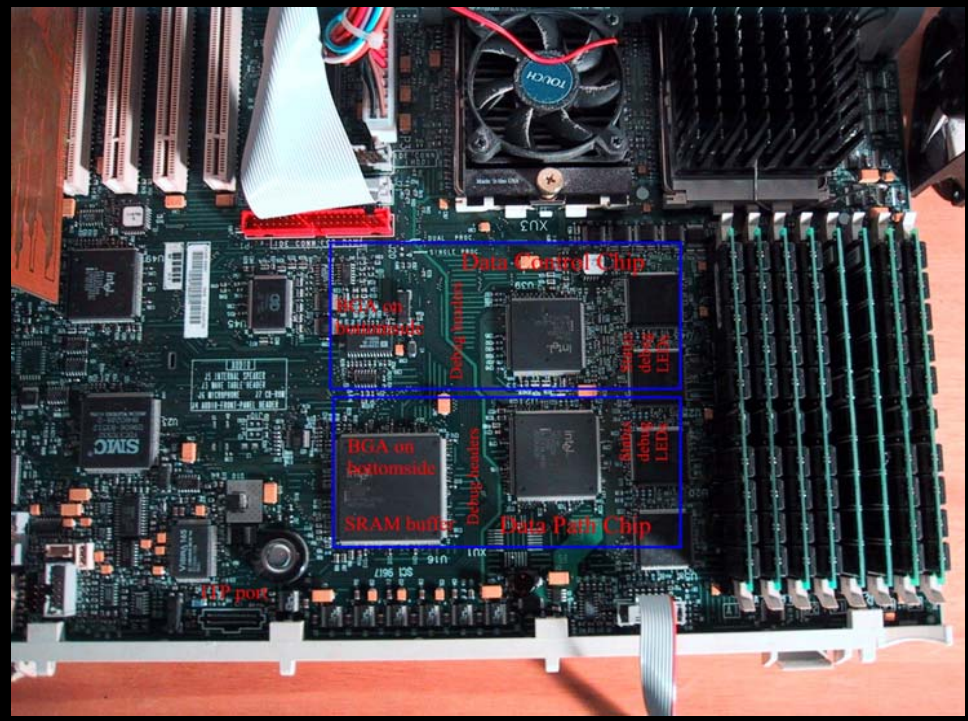


Sample ACE Results



Memory Flexible Interface

- Orion (450GX) Memory controller.
  - Synthesis complete, some simulation
  - Board ready to tapeout
- Chipset pre-fetch and memory studies



	Altera – Cyclone C12 (12K LE = ~200K gates)	Xilinx – Spartan3 S1500 (26.6K LUT = ~1.5M gates)
Estimated logic size	9K LE	8K LUT
Max Frequency	74MHz/13ns	69MHz/14ns
Estimated gate count	~150K	~480K

Programmable Memory Interface

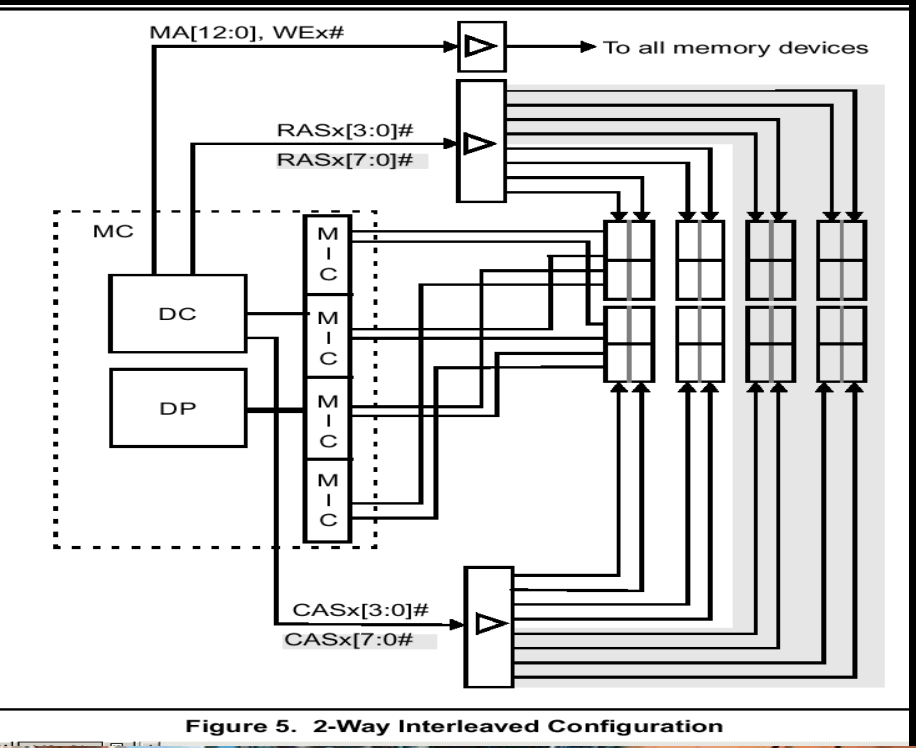
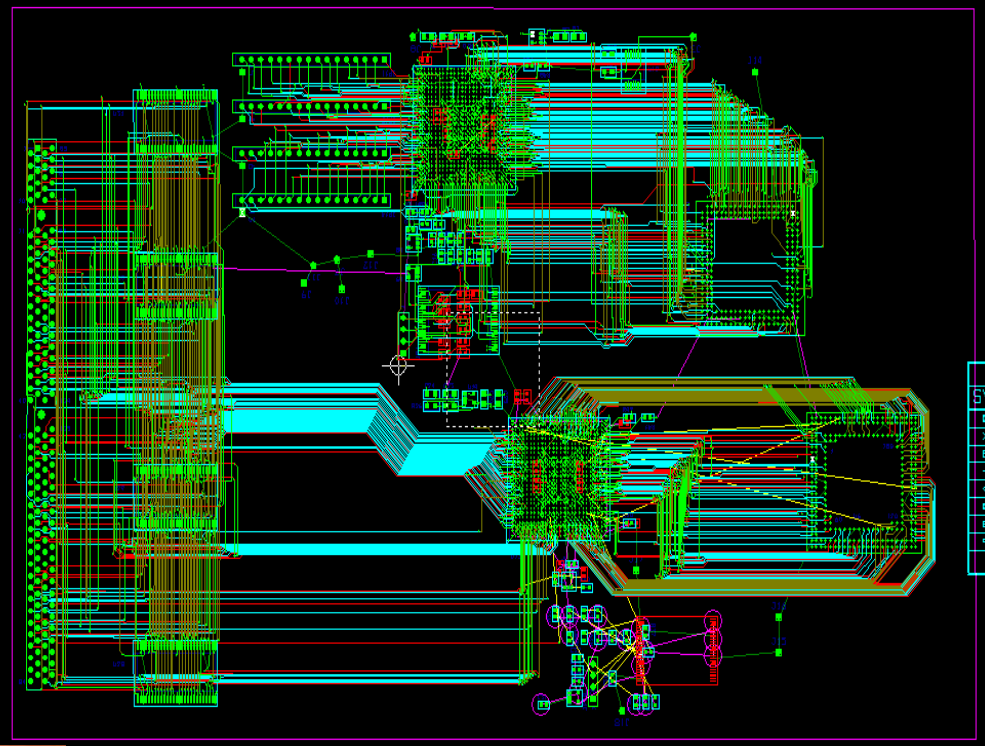
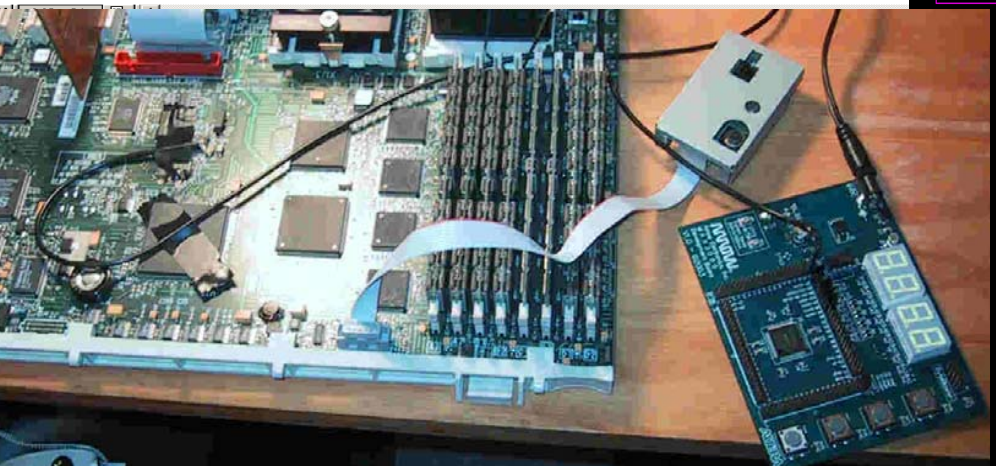
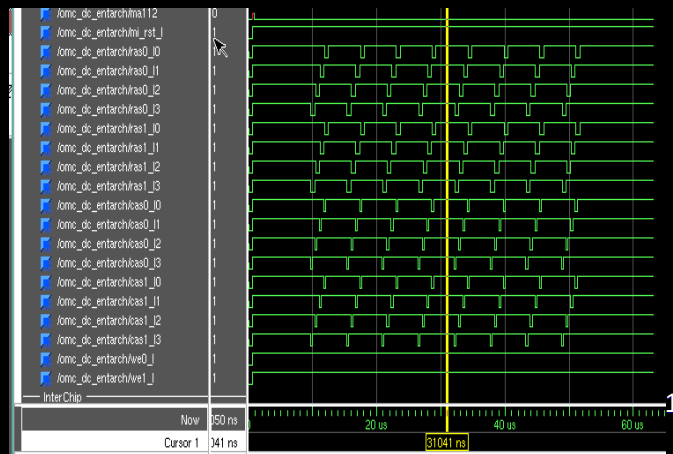


Figure 5. 2-Way Interleaved Configuration







Conclusion

- Target FPGA emulation on a more defined and specific area – memory subsystem
  - Some limitations
  - Easier to setup real workloads