A Flexible Architecture for Simulation and Testing (FAST) Multiprocessor Systems

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FAST @ Glance

- Custom PCB design
- 4-way tightly-coupled multiprocessor
- Real R3000/R3010 cores, CPU/FPU
- Flexible memory simulation hierarchy, including L1 caches
FAST Capabilities

- Real Applications
  - Including OS & FP-intensive code
- Multiprocessor systems up to 4 processors
- Variety of Memory Structures
  - L1 and/or L2 caches, FIFO’s, DRAM
- Emulation of on-chip and off-chip memory latencies
- Expandable interface
  - Multiple PCBs, other digital interfaces
FAST Simulation Space

• Thread Level Speculation
  – Stanford’s HYDRA CMP

• Transactional Memory
  – Stanford’s TCC

• Large-Scale Networked CMP
  – Stanford’s Smart Memories

• Multithreaded HW

• Embedded SOC Architectures

• All at multi-MHz speeds
FAST Processor Tiles

- 4 MIPS-based Processor Tiles
- CPU and FPU
  - External Cache and Coprocessor interface
- Local Memory Controller
  - Cache or other memory structures
- Coprocessor
  - Additional Functionality
  - ISA Extensions
- L1 Local Memory
  - SRAMs: 256K X 36-bit
MP FAST

• Read/Write Controller:
  – Hub of the multi-core system
  – Handles the interprocessor interaction

• Shared Memory Controller:
  – Interfaces the RWC with the L2 memory SRAM array and the expansion connector
  – Expansion connector can connect multiple PCBs, main memory daughter card, or other digital interfaces.
FAST Support HW

• Host communication
  – Daughter card with embedded processor and Ethernet controller

• CPLD
  – FPGA Programming
  – Clock Management
  – PCB Management

• Flash Memory
  – Store FPGA bitstreams
  – Onboard SW, like Board OS
FAST Conclusions

- Flexible hardware emulation platform for tightly-coupled multiprocessor systems
- Emulate a variety of memory systems
- Full system or partial system simulation
- Expandable simulation fabric
- Integer and Floating-point applications
BACKUP
Complete FAST
FAST HW at a Glance

- 4 MIPS-based Processor Cores:
  - CPU and FPU @ 25MHz
  - 2 XCV1000 @ 25-100MHz
  - L1 Local Memory, each: 256K X 36-bit @25-100MHz
- XC2V6000 L2 Shared Memory Controller @ 200 MHz
  - 16M X 36-bit L2 Shared Memory @ 200 MHz
- XC2V6000 Read/Write Controller @ 200 MHz
- All on PCB I/O @ 3.3V
- Three main clock domains: 25MHz, 100MHz, 200MHz
- Four voltage domains: 1.5V, 2.5V, 3.3V, 5.0V
- 128Mb Flash Memory to store FPGA configurations and PMON OS
- CPLD for additional control, FPGA programming, etc.
- RCM3200 Microcontroller with Embedded Ethernet Port for off-PCB Communication
FAST PCB Details

- 23 Layer Board
- 4200 nets
- 28000 vias
- 43 BGA packages
- 2500 testpoints
- 4300 parts
FAST Status

- PCB in fabrication and assembly phase
- Need to partition Verilog for initial Speculative Thread design
- Building Morphware infrastructure for Rapid prototyping