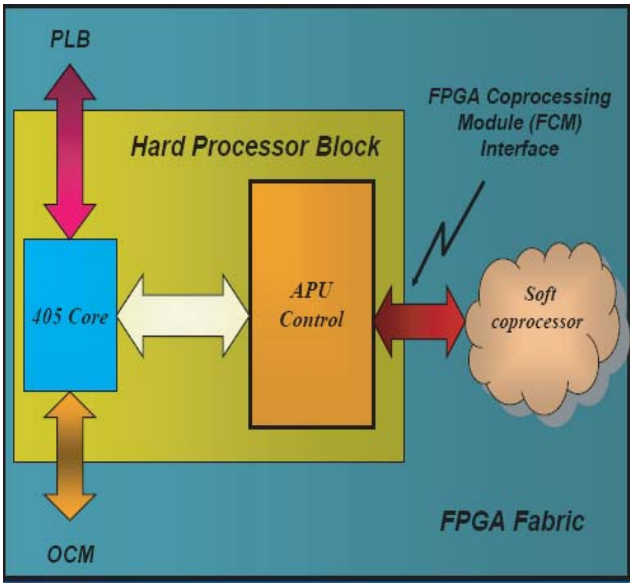
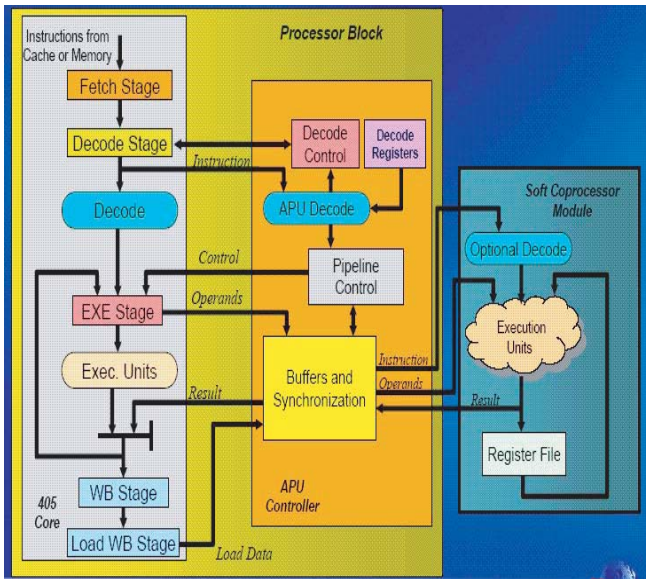
Accelerated System Performance with APU-Enhanced Processing

The Auxiliary Processor Unit (APU) controller is a key embedded processing feature in the Virtex-4 FX family.

- Achieve significant performance improvement with Virtex-4 FX Family
- Gain flexibility utilizing User Defined Instructions to extend PowerPC ISA
- Leverage PowerPC high bandwidth, low latency APU interface
- Simplify HW/SW partitioning tasks

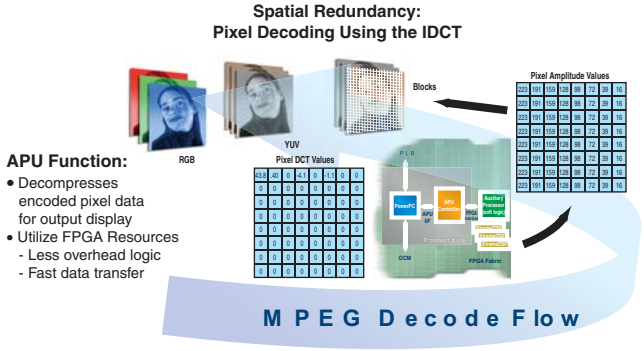


Top Level APU Control Module Interface



APU Control Interaction Flow Diagram

APU manages all interactions between PowerPC405 soft co-processor in FPGA
- Directly couples PowerPC and hardware accelerators in FPGA logic
- Synchronizes soft Co-Processing Module, Operates at CPU frequency



APU Function:
- Decompresses encoded pixel data for output display
- Utilize FPGA Resources
  - Less overhead logic
  - Fast data transfer

- Leverages Virtex-4 Integrated Features
  - > Embedded PowerPC
  - > Integrated APU Controller
  - > Extreme DSP Blocks
- High Bandwidth Low Latency Interface
- Efficient HW/SW Design Partitioning
- Significant performance improvement

20X vs. SW Emulation

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