

Toward A Common Emulation Infrastructure with Large-Scale FPGA

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Introduction

- The diversification of processor architectures and applications result in long simulation time when using **detailed software simulators**.

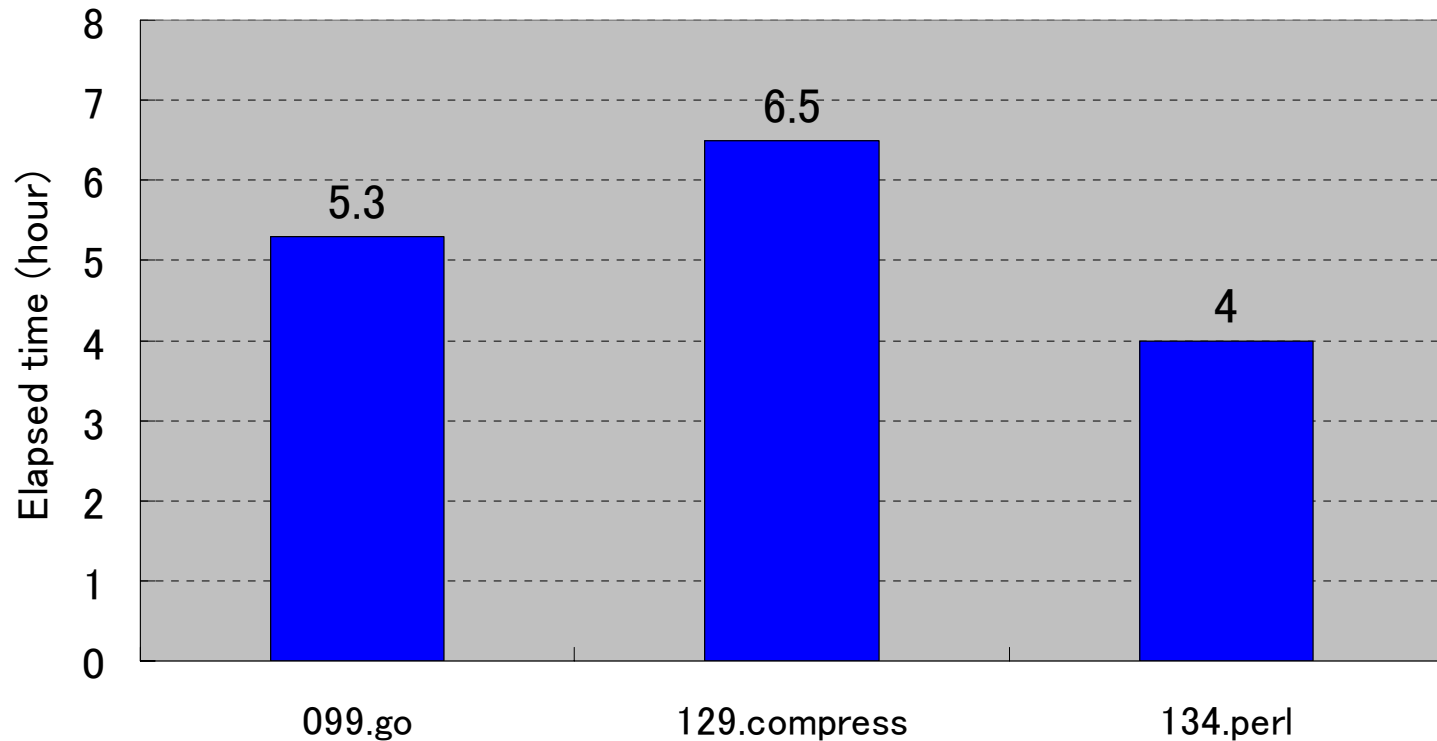
Table 1: Simulation speed of sim-cache.

| Program | inst | Time | inst/sec |
|--------------|------------|----------|--------------|
| 099.go | 35 billion | 5.3 hour | 1.88 million |
| 129.compress | 43 billion | 6.5 hour | 1.82 million |
| 134.perl | 24 billion | 4.0 hour | 1.66 million |

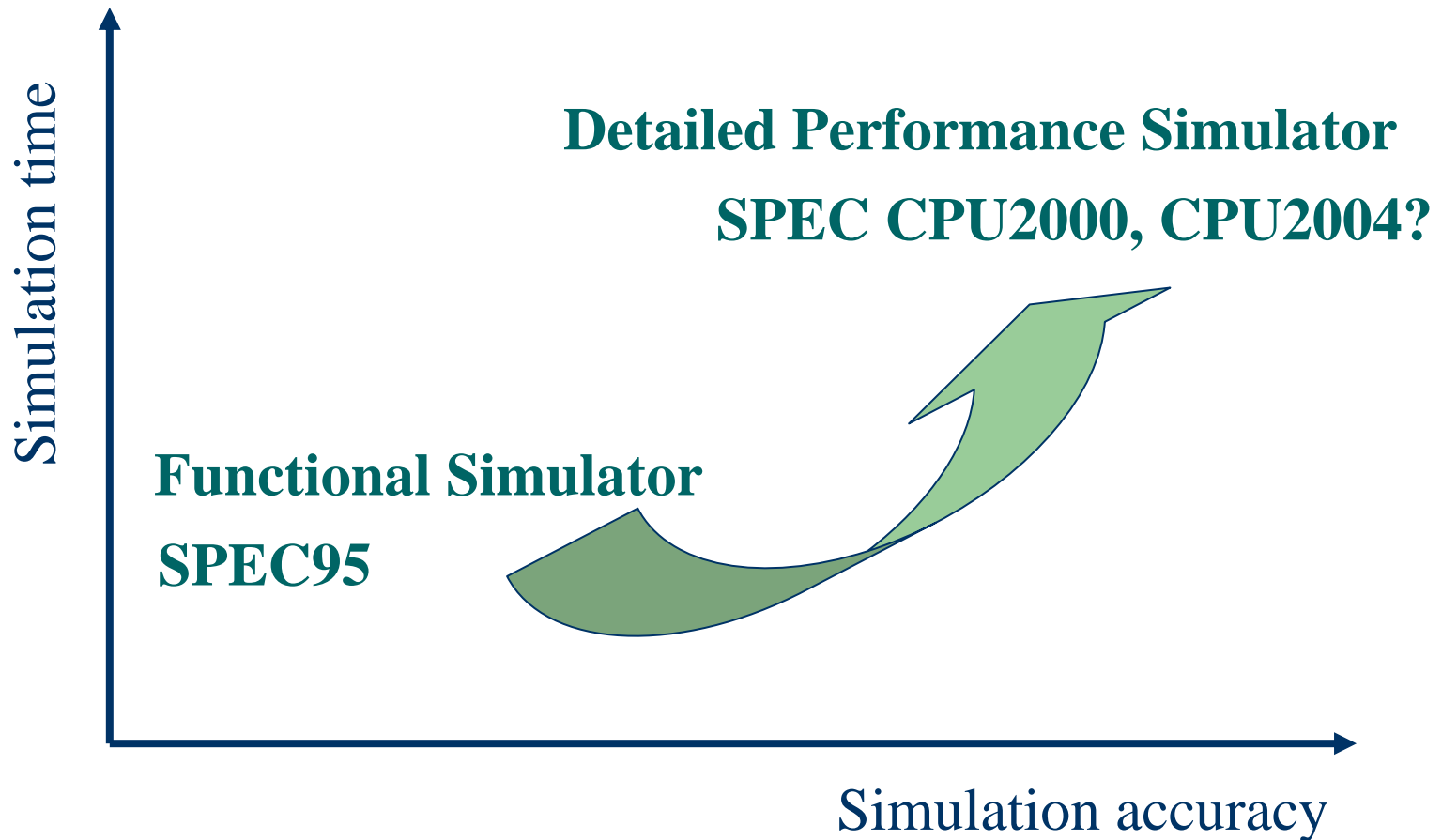
On a computer with Pentium III Xeon 700MHz

Simulation speed of sim-cache

- DELL PowerEdge 6400/700 (Pentium III Xeon 700MHz)
- SimpleScalar Tool Set (sim-cache), SPEC CPU95



Limit of slow software simulators

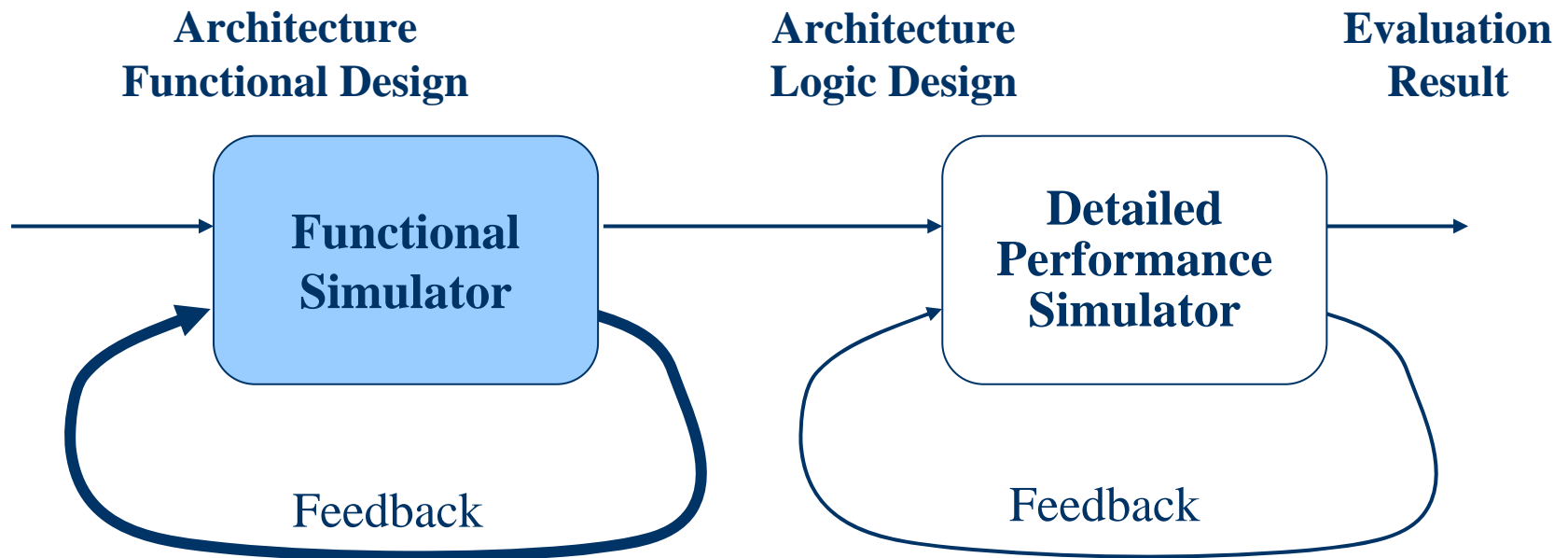


Purpose

- The major research goal of our project is to build a **common hardware platform to emulate various processor architectures.**
- We are developing a hardware emulation **infrastructure** with large-scale FPGA.
 - Our first target is a fast and flexible cache system emulation.

Flow in a microprocessor design process

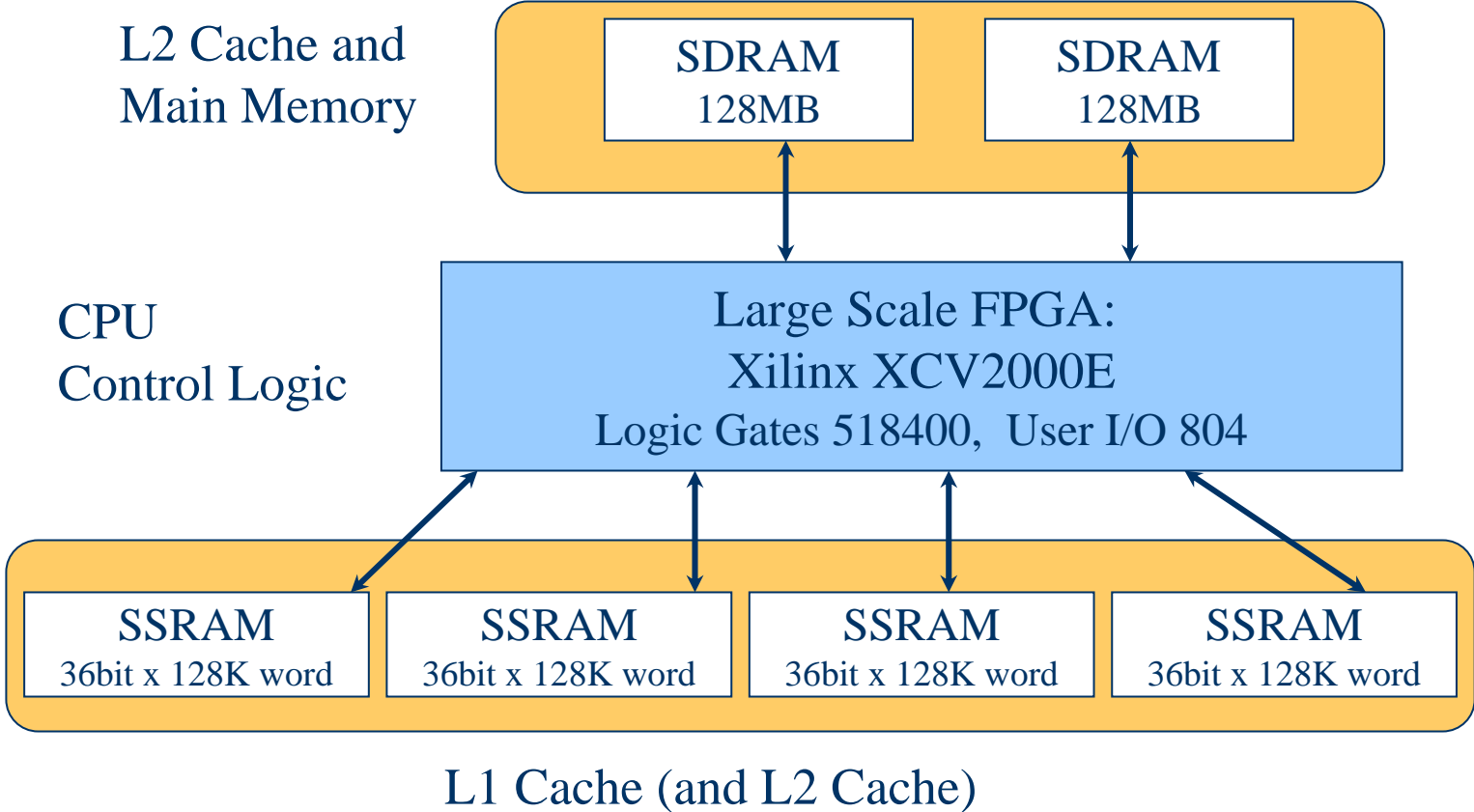
- Functional simulators are used in the early phase of the design process.
- Then detailed performance simulators are used.
- We tries to shorten the simulation time of the first phase.



Hardware emulation with FPGA

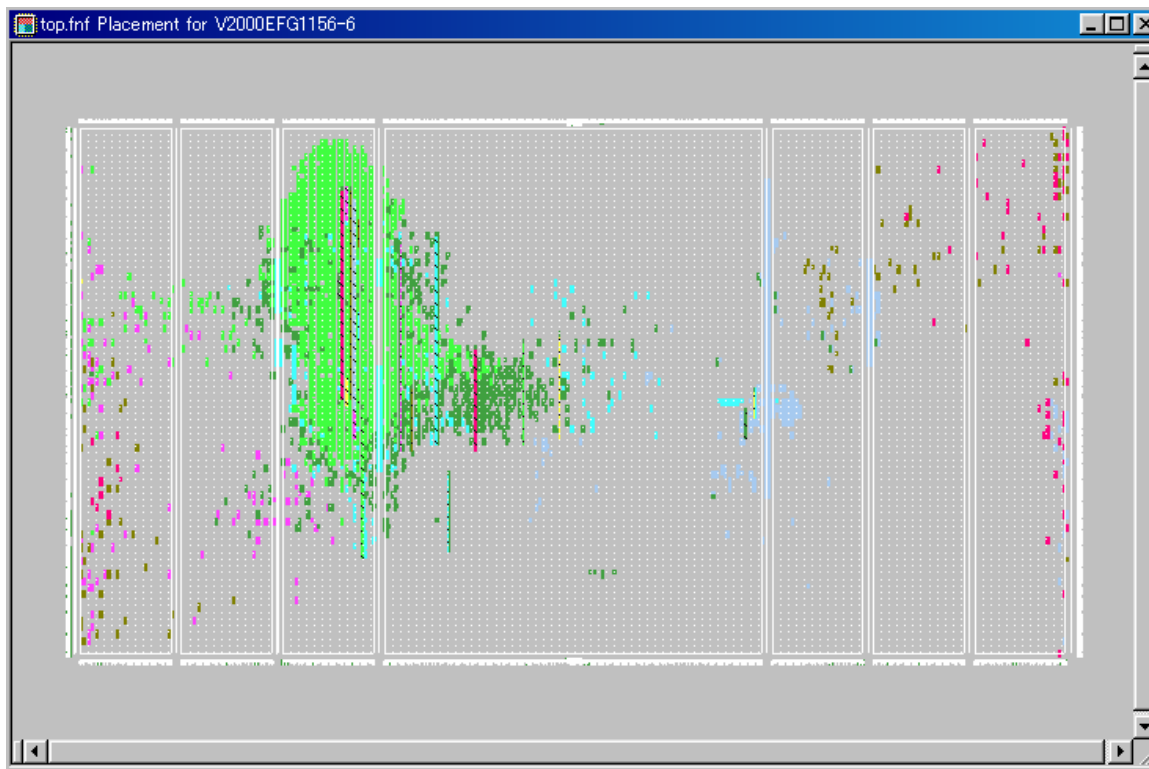
- Our target clock speed of the system is **40MHz**.
- If a processor on FPGA achieves IPC (instructions per second) of 1 with the pipelining, the total throughput of the hardware emulation achieves **40 MIPS** (million instructions per second).
- This is **20 times faster** than a software simulator sim-cache of about 2 MIPS.

Block diagram of a hardware emulator



A placement result for V2000EFG1156

We are developing an Alpha processor core and cache systems on a FPGA board. This version of processor core has no floating-point register and unit. It is written in Verilog-HLD and synthesized with Xilinx Foundation ISE.



Even if a 64-bit processor core is implemented, it occupies only 12% of the hardware resources. We confirmed that the clock speed of current implementation is 30MHz.

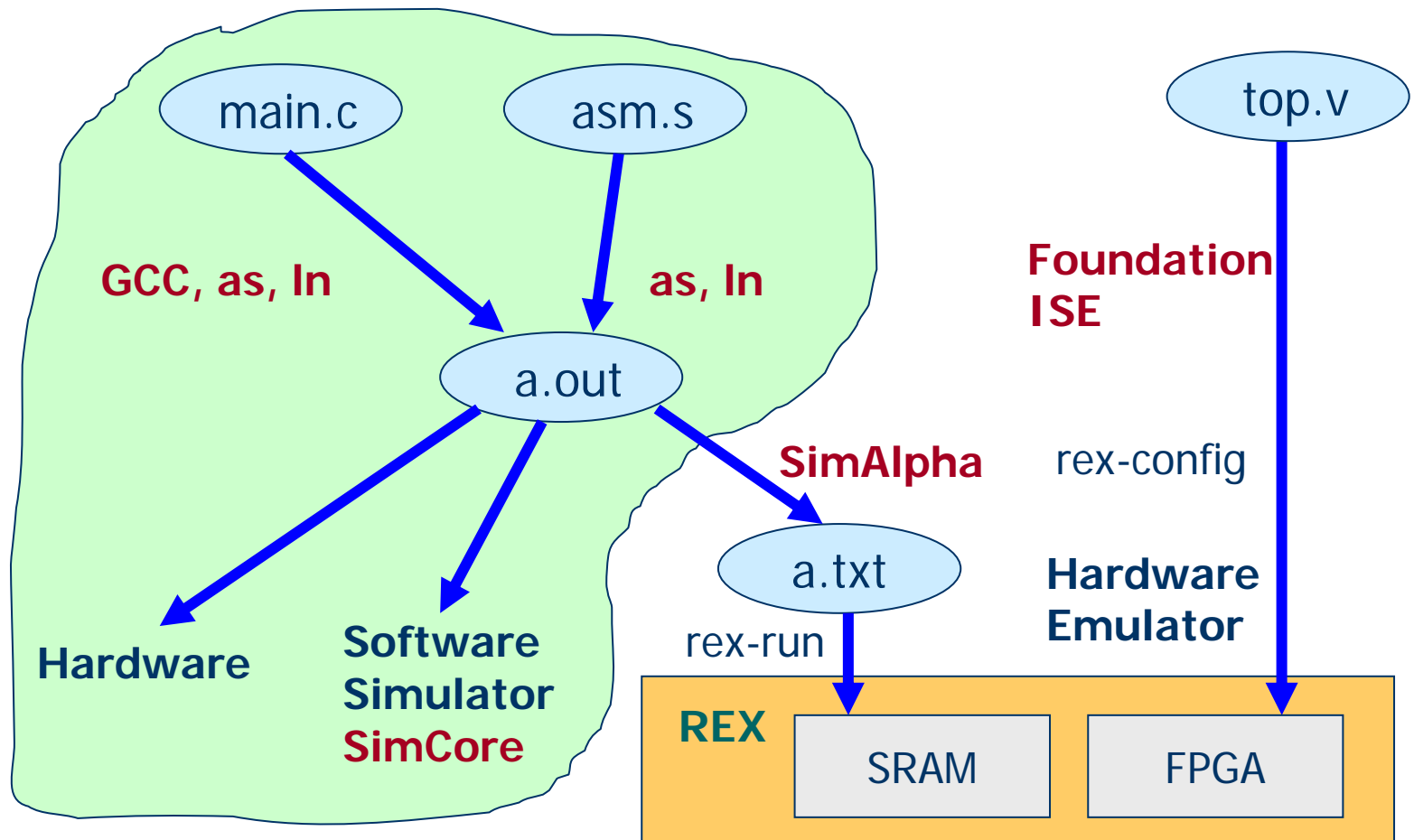
FPGA board REX



REX
(Reconfigurable
EXperiment
equipment)



System overview



Present status and future plan

- We are developing an Alpha processor core and cache systems on a FPGA board.
 - 12% of the hardware resources
 - 30MHz frequency
- Our future plan includes an efficient (**simple**) implementation of **system calls** in order to run SPEC CPU benchmark.