Introduction to the Raw Handheld Board

Jason Miller, David Wentzlaff, Nathan Shnidman
Presentation Outline

- Raw’s I/O ports (basic)
- Memory sub-system
- PCI and host PC connection
- Expansion interface
- Integrated peripherals and connectors

- Raw’s I/O ports (detailed)
Raw Chip I/O Ports

I/O Multiplexing:
- Drop ST2
- Round-robin arbitration for MDN, GDN and ST1
- Ports 01 & 02 and ports 09 & 10 are merged
- 14 ports total
- May be numbered in hex
- Each port is actually separate input and output busses
Let’s start building a Raw board

- Single Raw processor
- 14 I/O ports
Add a memory sub-system

- 2 Xilinx XC2V3000 FPGAs for memory controllers
- Separate memory controller on each port
- 512 MB PC133 SDRAM DIMM for each controller
- 128 MB address space for each tile by default
Add a PCI sub-system

- Xilinx XC2V3000 FPGA for PCI controller
- Three 64-bit / 66 MHz PCI slots
Add a PCI sub-system

- Xilinx XC2V3000 FPGA for PCI controller
- Three 64-bit / 66 MHz PCI slots
- Xilinx XC2V1000 FPGA for Config
- “Backdoor interface” for connection to host PC
Add an expansion interface

- Xilinx XC2V3000 FPGAs for LE and RE
- 190-pin MICTOR connectors for general use
Finally, some I/O interfaces

- Xilinx XC2V3000 FPGA for controllers
- Various integrated devices and connectors
Integrated I/O and Connectors

- Audio frequency ADCs and DACs
  - 2 channels, up to 44.1 kHz, 16-bit samples, RCA jacks
- High-speed analog to digital converter
  - Up to 100 MHz, 12 bit precision, SMB connector
- Serial (RS-232) port w/ 16550 UART
  - 9-pin D-SUB connector
- PS/2 keyboard port (controller in FPGA)
- LCD connector
  - 4x40 character, text-only LCD display: Optrex DMC-40457
- Daughter-card connector
  - Planned: 100 Mbit Ethernet and USB 2.0 controllers
  - 50 signal pins, 66 MHz clock, 5V and 3.3V power
Raw Fabric System

2x2 Raw Board

Peripheral Board
Raw Fabric System (cont)
Raw I/O Ports (detailed)
Raw I/O Ports (detailed)
Raw I/O Ports (detailed)

Sending Tile

Network Switch

Receiving Tile

Data Valid Thanx SIB

Network Switch

1
Raw I/O Ports (detailed)

Sending Tile

Network Switch

Receiving Tile

Data
Valid
Thanx
SIB

Sending Tile

Network Switch

Receiving Tile

Data
Valid
Thanx
SIB

32 Data Out
2 Ready Out
Yummy S In
Yummy M In
Yummy G In

32 Data In
2 Ready In
Yummy S Out
Yummy M Out
Yummy G Out

Normal Port:
2 Ready bits
3 Yummy bits

Ready Encodings
00 = None
01 = Static
10 = Memory
11 = General

Double Port:
3 Ready bits
6 Yummy bits

Ready Encodings
000 = None
001 = Static Port 1
010 = Memory Port 1
011 = General Port 1
100 = None
101 = Static Port 2
110 = Memory Port 2
111 = General Port 2