Synchronous Communication Techniques for Rationally Clocked Systems

by

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Abstract

An increasingly common problem in designing high-performance computer systems today is that of achieving efficient communication between systems running at different clock speeds. This problem occurs, for example, in uniprocessor systems where the processor runs faster than the bus, and in heterogenous multiprocessor systems where processors of different kinds run at their own maximum speeds. Asynchronous solutions to this problem, which assume the systems' clocks to be completely independent, are typically inefficient because they must allow for sufficiently long synchronization delays to attain acceptable levels of reliability. Synchronous solutions, on the other hand, though more efficient and reliable, have traditionally lacked flexibility because they require the clock frequencies to be related by integer factors.

An efficient and flexible synchronous solution, called rational clocking, has been proposed that permits data to be transferred reliably and efficiently between two systems whose clock frequencies are related by the ratio of two small integers. This rational frequency constraint allows a wide variety of frequencies to be used, and at the same time assures a periodic relationship between the two clocks that can be used to determine a schedule for data transfers between the two systems.

In this thesis we present, improve, and test the rational clocking technique. We begin with the original table-based implementation, where the communication schedules are pre-computed and stored in lookup tables, and discuss some minor variations and improvements. Then, we improve the throughput of this technique with a double-buffering technique that guarantees 100% throughput efficiency for all frequency ratios and timing parameters. We also improve the space-efficiency and flexibility of the scheduling hardware dramatically by using a set of run-time scheduling algorithms that do not require lookup tables. Finally, we test all these ideas using a combination of software and hardware tools, including scheduling software, Verilog simulations, and a custom-designed CMOS VLSI chip.

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