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More parallelism, less overhead

• Mainstream microarchitectures are currently designed to minimize compiler’s impact
  – most of the power and chip area spent in buffering and scheduling
  – less than 20% of the power is for actual execution
  – even less of the chip area is for actual execution

• In the next decade, new applications will demand
  – much better performance, power and cost
  – VDSL, software radio, pervasive networking, high-speed switches

• Compiler-enabled architectures for DSP and embedded:
  – long-term competitiveness though reprogrammability
  – performance scalability though partitioning
  – power savings through more locality and slower clocks
  – design-time reduction by reusing general hardware
Example: VDSL CAP Receiver

• VDSL not viable on today’s DSP
  – Execution units
  – Memory bandwidth

• Future:
  – Exploit algorithmic locality in a scalable architecture
  – Use compiler to partition memory access and computation
VDSL in a scalable-interface VLIW DSP

- Statically scheduled VLIW architecture
  - Compiler partitions computation and associated memory reference and storage
  - Centralized control with shift interconnect designed to hot-path common merges
  - Compiler managed multi-threading/streaming with real-time guarantees
  - Seamless interface to special function blocks
- 2000 MACs sustained with 16 units at lower power than current VLIW DSPs
Enabling compiler technology

• Deep program analysis
  – High-resolution data flow
  – Pointer / alias / array/ structure reference analysis
  – Advanced control flow manipulation techniques
  – Software / architecture power modeling
  – Safe execution time analysis
  – Identify opportunities for parallel execution and partition data set

• Parallelization and optimization
  – Computation and memory reference partitioning
  – Localization of memory and instruction references
  – Efficient, low-overhead multithreading with real-time guarantees
  – Managing specialized and/or non-uniform architectures
Most Important Microprocessor of 2010

• No single most important microprocessor
• Where will be the most exciting growth be?
• Domain Specific Processors that drastically
  – reduce needs for ASIC’s
  – increase performance per watt
  – increase performance per mm²
  – improve real-time characteristics