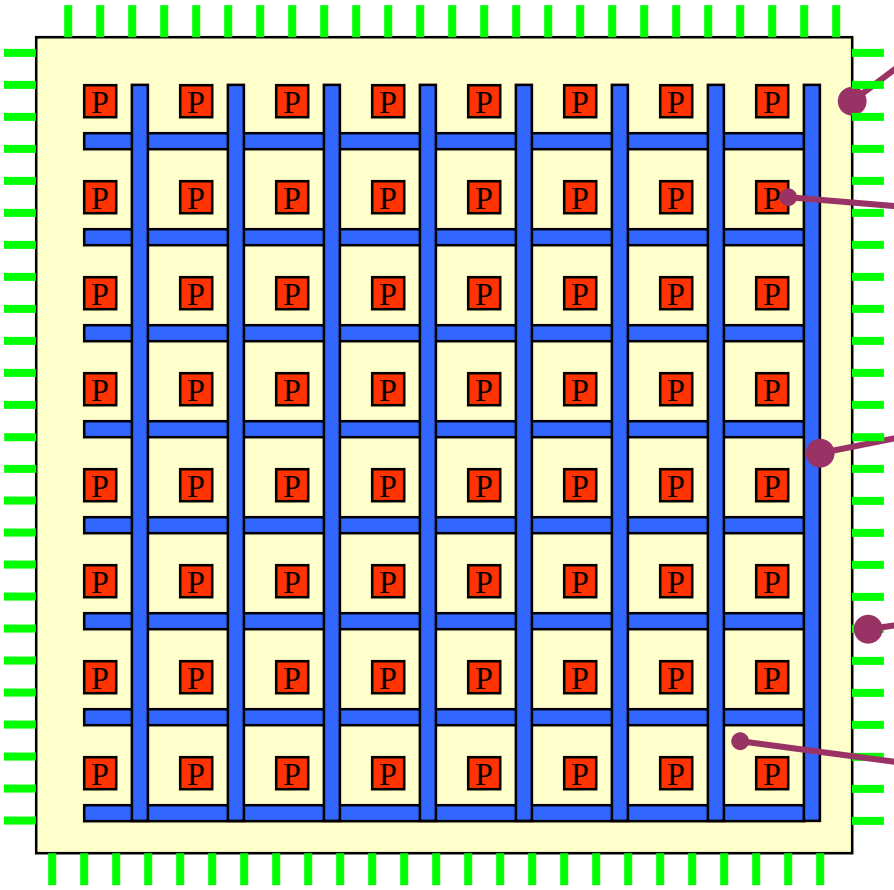
100x μP performance by 2010
32x Parallelism, 2.5x process, 1.25x gates/ck



2010 μP chip, 0.07μm CMOS
10^5 tracks/side => 10^{10} grids

64 dual-issue 64b FP μPs
2GHz, 4GFLOPs, 10^7 grids

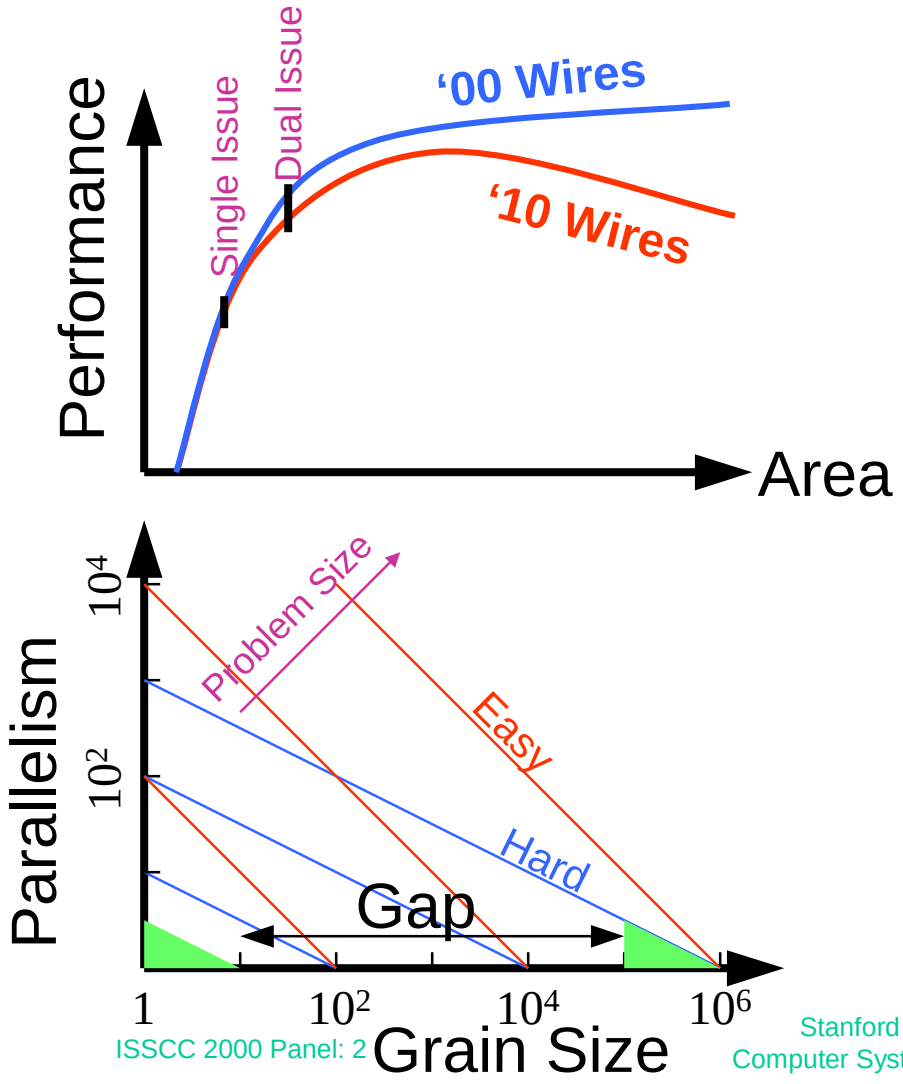
On-chip network
16Tb/s bisection

Pinout, 500 pairs at 10Gb/s
5Tb/s off-chip BW

4Gb of RAM

(Data from 1999 ITRS)

Explicit Parallelism
Explicit Communication



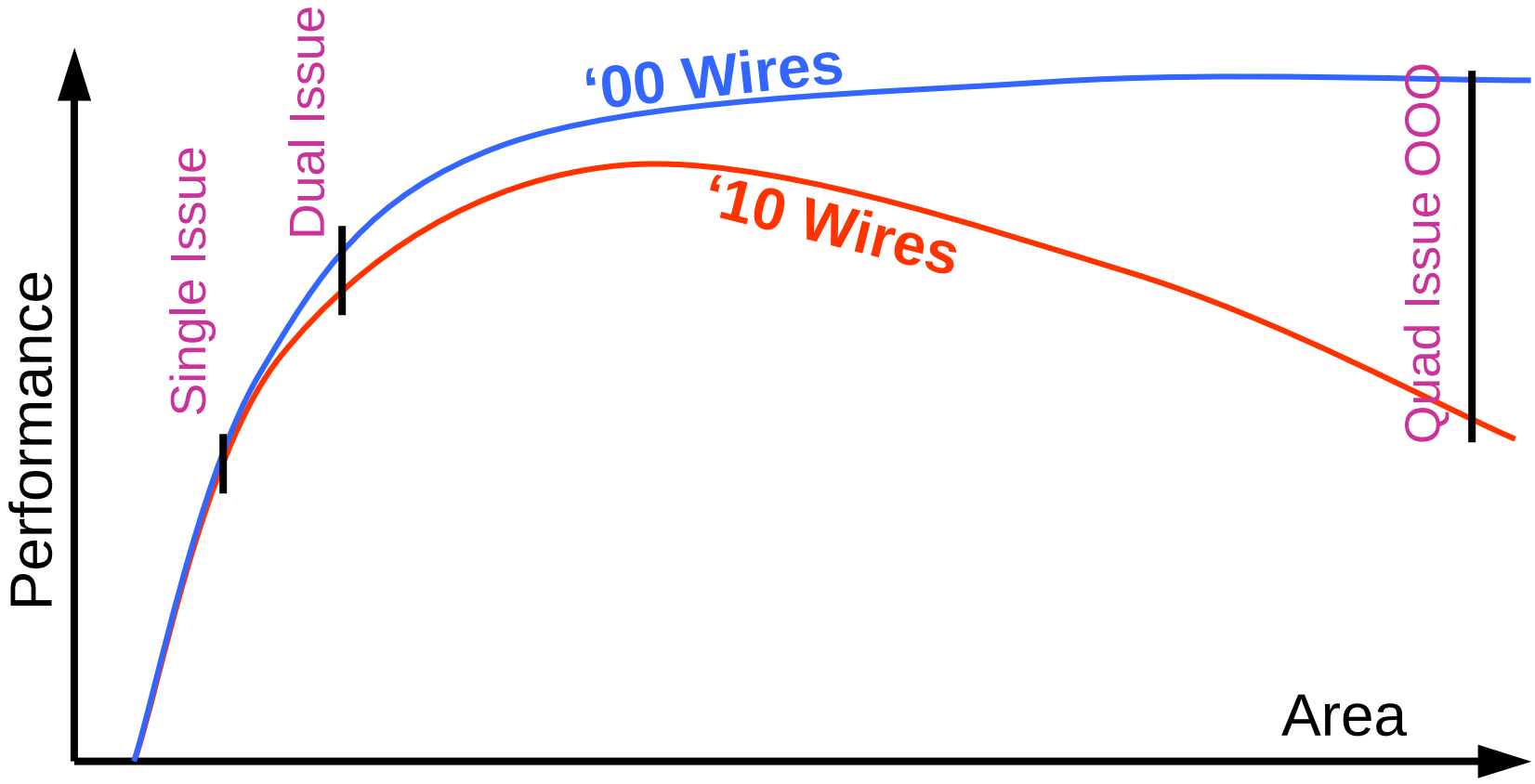
Slow wires reduce already diminishing returns from 'hero' processors

Lots of parallelism in all demanding problems

Fast communication and synchronization mechanisms close the parallelism gap

Communication, not arithmetic is the scarce resource. Explicit communication

Slow Wires accelerate already diminishing returns of implicitly parallel processors



Lots of parallelism in demanding problems
Fine-grain comm and sync mechanisms expose it