Panel Discussion: Grand Ballroom: 6-10PM

Topic: How to compute with a billion transistors on a chip

Our opinionated, fun, and visionary panelists will argue about the "right way" to do so, probably covering multi-threading, status quo, super speculation, simultaneous multithreading, on-chip multiprocessors, reconfigurable computing, processors in memory, and abacuses on a chip. The panelists are:

Tom Knight, MIT
Hank Levy, University of Washington
John Moussouris, Microunity, Inc.
Bob Parker, DARPA
David Patterson, University of California, Berkeley
Kunle Olukotun, Stanford
Guri Sohi, University of Wisconsin
Moderator: Anant Agarwal, MIT

Friday, October 4

Compiler Optimizations: 9:00-10:30
David Wall, Silicon Graphics, Inc.

Compiler-Based Prefetching for Recursive Data Structures, *Chi-Keung Luk and Todd C. Mowry: University of Toronto*

Exploiting Dual Data-Memory Banks in Digital Signal Processors, *Mazen A. R. Saghir, Paul Chow and Corinna G. Lee: University of Toronto*

Compiler-Directed Page Coloring for Multiprocessors, *Edouard Bugnion, Jennifer M. Anderson: Stanford University, Todd C. Mowry: University of Toronto, Mendel Rosenblum and Monica S. Lam: Stanford University*

Caches and Memory Systems: 11:00-12:30
Garth Gibson, Carnegie Mellon University

Reducing Network Latency Using Subpages in a Global Memory Environment, *Herve A. Jamrozik, Michael J. Feeley, Geoffrey M. Voelker, James Evans II, Anna R. Karlin, Henry M. Levy and Mary K. Vernon: University of Washington*

Improving Cache Performance with Balanced Tag and Data Paths, *Jih-Kwon Peir: University of Florida, Windsor W. Hsu: University of California at Berkeley, Honesty Young and Shauchi Ong: IBM Almaden Research Center*

Operating System Support for Improving Data Locality on CC-NUMA Compute Servers, *Ben Verghese, Scott Devine, Anoop Gupta and Mendel Rosenblum: Stanford University*

Lunch: East Room and Charles Suite: 12:30pm-2pm

Tutorial-4, Somerset Room: 1:30pm-5pm , Decoupled Processing: Past, Present, and Future. (M. Farrens & G. Tyson) (http://cag-www.lcs.mit.edu/asplos7)

Tutorial-5, University A Room: 1:30pm-5pm: Efficient Implementation of Object-Oriented Languages. (C. Chambers) (http://cag-www.lcs.mit.edu/asplos7)

Saturday, October 5

Registration: Charles suite Foyer

Workshop-2: Sixth Workshop on Scalable Shared Memory Multiprocessors: Charles suite *(http://www-csag.cs.uiuc.edu/asplos/scalable-sm.text)*

Lunch: East Room

Conference Chairs

General: Bill Dally, MIT
Program: Susan Eggers, University of Washington
Tutorials and Workshops: Andrew Chien, Univ. of Illinois
Treasurer: Randy Osborne, Mitsubishi Electric ITA
Publicity: Robert Bedichek, Transmeta Corp.
Local Arrangements: Jamey Hicks, Digital CRL
Registration: Marco Fillo, Digital

Program Committee

Anant Agarwal, MIT
Tom Anderson, UC Berkeley
Mary Baker, Stanford University
John Bennett, Rice University
Craig Chambers, University of Washington
Ron Cytron, Washington University
Garth Gibson, Carnegie Mellon University
Wen-Mei Hwu, University of Illinois
Frans Kaashoek, MIT
Kathryn McKinley, University of Massachusetts
Susan Owicki, Independent Consultant
Larry Peterson, University of Arizona
Dick Sites, Digital SRC
Mike Smith, Harvard University
Per Stenstrom, Chalmers University of Technology
David Wall, Silicon Graphics Inc.
David Wood, University of Wisconsin
Ben Zorn, University of Colorado

Conference Site and Accommodations

The Royal Sonesta Hotel is located in Cambridge, Massachusetts, on the banks of the Charles River and overlooking Boston's famed Beacon Hill. The hotel is only minutes from MIT, Harvard, Government Center, and Cambridge High Tech Centers. The Sonesta has easy access to the historic waterfront, Quincy Market and the financial district.

Air Transport: The nearest airport is Boston Logan airport.
Ground Transport: One can take a taxi (around $15) or the T (subway) from Logan airport to the hotel. Accommodations: The Royal Sonesta Hotel, 5 Cambridge Parkway, Cambridge, Massachusetts 02142, Call 617-491-3600 for reservations (mention ASPLOS). Reservations must be made before August 30, 1996 in order to guarantee room availability and rates. Single and double rooms are both $149.00 per night. There is an additional $20.00 charge for each additional person in the room per night.

Registration Instructions

Conference registration includes one copy of the proceedings, lunches, breaks and receptions. Registration for the tutorials includes one copy of notes, lunch, and breaks. Registration for the Workshops and Tutorials can only be accepted in conjunction with conference registration. The student registration fee excludes meals and receptions. Student Registration must include a copy of a valid full-time student ID. Completed Registration must be mailed to:

AP Conventions
c/o Leah Forte (ref: ASPLOS-VII)
185 Devonshire Street
10th Floor
Boston, MA 02110, U.S.A.

Fax.: +1 (617) 350-7359, Tel.: +1 (617) 350-0080

Early Registration must be postmarked by **August 31st, 1996.** Full payment in U.S. dollars must accompany registration: check drawn on U.S. bank or Money order in U.S. dollars made payable to ACM ASPLOS VII , or charge to a MasterCard, Visa or American Express card. Credit card registration may be faxed.

To cancel early (before **August 31st)** registration, a request in writing must reach the above address before **September 7th, 1996.** The full registration fee, less U.S.$50 in processing charges, will be refunded. No refund is available for cancellation of late (after August 31st) or on-site registration.

ASPLOS-VII Registration Form

http://www.ai.mit.edu/people/fillo/asplos/reg.html

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Affiliation__________________________________
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Please list any special needs__________________
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Circle your choices.

Before 8/31/96	**non-member**	**member**	**student**
Conference:	$425	$325	$150
Tutorial-1:	$150	$125	$50
Tutorial-2:	$150	$125	$50
Tutorial-3:	$150	$125	$50
Tutorial-4:	$150	$125	$50
Tutorial-5:	$150	$125	$50
Workshop-1:	$150	$125	$50
Workshop-2:	$150	$125	$50
After 8/31/96	**non-member**	**member**	**student**
Conference:	$495	$395	$150
Tutorial-1:	$200	$150	$75
Tutorial-2:	$200	$150	$75
Tutorial-3:	$200	$150	$75
Tutorial-4:	$200	$150	$75
Tutorial-5:	$200	$150	$75
Workshop-1:	$200	$150	$75
Workshop-2:	$200	$150	$75

All tutorials are half-day. Tutorial-2 and Tutorial-3 are at the same time, as are Tutorial-4 and Tutorial-5)
__Money Order (in US $)__Check drawn on U.S. bank, payable to: ACM ASPLOS-VII
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Advance Program for

ASPLOS-VII

Seventh International Conference on

Architectural Support for Programming Languages and Operating Systems

October 1-5, 1996
Cambridge, Massachusetts

http://cag-www.lcs.mit.edu/asplos7

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Tuesday, October 1

Registration, 7:30am-5pm: Somerset Foyer

Workshop-1: Second NOW/Cluster Workshop: Building Systems of Systems, Riverfront 8:30am-5pm, (Organizers: Andrew Chien and David Culler) (http://www-csag.cs.uiuc.edu/individual/achien/asplos/now-cluster.html)

Tutorial-1, morning, Compiler and Architecture Support for Java, East Room: 8:30am-12pm, (Wen-mei Hwu) (http://cag-www.lcs.mit.edu/asplos7)

Lunch: Skyline ABCDE: 12-1:30pm

Tutorial-2, afternoon: Code optimization in Modern Compilers, Somerset Room: 1:30pm-5pm, (K. Palem & V. Sarkar) (http://cag-www.lcs.mit.edu/asplos7)

Tutorial-3, afternoon: Program Analysis and the Optimization at the Source Language Level, East Room: 1:30pm-5pm, (D. Padua) (http://cag-www.lcs.mit.edu/asplos7)

Welcome Reception at the Royal Sonesta, Riverfront Room 6-8PM

Wednesday, October 2

Registration, 8am-5pm: Grand Ballroom Foyer
Sessions 9am-5:30pm: Grand Ballroom

Welcome and Multiprocessors: 9:00-10:30
David Wood, University of Wisconsin at Madison

The Case for a Single-Chip Multiprocessor, *Kunle Olukotun, Basem A. Nayfeh, Lance Hammond, Ken Wilson and Kunyung Chang: Stanford University*

An Evaluation of Memory Consistency Models for Shared-Memory Systems with ILP Processors, *Vijay S. Pai, Parthasarathy Ranganathan, Sarita V. Adve and Tracy Harton: Rice University*

More Multiprocessors: 11:00-12:00
David Wood, University of Wisconsin at Madison

Synchronization and Communication in the T3E Multiprocessor, *Steven L. Scott: Cray Research, Inc.*

Evaluation of Architectural Support for Global Address-Based Communication in Large-Scale Parallel Machines, *Arvind Krishnamurthy: University of California at Berkeley, Klaus E. Schauser, Chris J. Scheiman: University of California at Santa Barbara, Randolph Y. Wang, David E. Culler and Katherine Yelick: University of California at Berkeley*

Lunch: East Room and Charles Suite 12pm-1:30pm

Threads: 1:30-2:30
Tom Anderson, University of California at Berkeley

Whole-Program Optimization for Time and Space Efficient Threads, *Dirk Grunwald: University of Colorado at Boulder and Richard Neves: IBM T.J. Watson Research Center*

Thread Scheduling for Cache Locality, *James Philbin, Jan Edler: NEC Research Institute, Otto J. Anshus: University of Tromso, Craig C. Douglas: IBM T.J. Watson Research Center and Kai Li: Princeton University*

File and Storage Systems: 3:00-4:00
Frans Kaashoek, Massachusetts Institute of Technology

The Rio File Cache: Surviving Operating System Crashes, *Peter M. Chen, Wee Teck Ng, Subhachandra Chandra, Christopher Aycock, Gurushankar Rajamani and David Lowell: University of Michigan*

Petal: Distributed Virtual Disks, *Edward K. Lee and Chandramohan A. Thekkath: Digital SRC*

Memory Requirements: 4:30-5:30
Ben Zorn, University of Colorado at Boulder

A Quantitative Analysis of Loop Nest Locality, *Kathryn S. McKinley: University of Massachusetts and Olivier Temam: Versailles University*

The Intrinsic Bandwidth Requirements of Ordinary Programs, *Andrew S. Huang and John Paul Shen: Carnegie Mellon University*

Banquet 6:30-10:30PM at the Museum of Science West Wing

Thursday, October 3

Registration: 8am-5pm: Grand Ballroom Foyer
Sessions: 9am-5:30pm: Grand Ballroom

Value and Branch Prediction: 9:00-10:30
Mike Smith, Harvard University

Multiple-Block Ahead Branch Predictors, *Andre Seznec: IRISA, Stephan Jourdan, Pascal Sainrat: IRIT and Pierre Michaud: IRISA*

Analysis of Branch Prediction Via Data Compression, *I-Cheng K. Chen, John T. Coffey and Trevor N. Mudge: University of Michigan*

Value Locality and Load Value Prediction, *Mikko H. Lipasti, Christopher B. Wilkerson and John Paul Shen: Carnegie Mellon University*

Potpourri: 11:00-12:00
Garth Gibson, Carnegie Mellon UniversityUniversity

The Structure and Performance of Interpreters, *Theodore H. Romer, Dennis Lee, Geoffrey M. Voelker, Alec Wolman, Wayne A. Wong, Jean-Loup Baer, Brian N. Bershad and Henry M. Levy: University of Washington*

Adapting to Network and Client Variability via On-Demand Dynamic Distillation, *Armando Fox, Steven D. Gribble, Eric A. Brewer and Elan Amir: University of California at Berkeley*

Lunch: East Room and Charles Suite: 12pm-1:30pm

Work-in-Progress and Outrageous Opinions: 1:30-3:00
Kathryn McKinley, University of Massachusetts at Amherst

Distributed Shared Memory: 3:30-5:30
John Bennett, Rice University

Shasta: A Low Overhead, Software-Only Approach for Supporting Fine-Grain Shared Memory, *Daniel J. Scales, Kourosh Gharachorloo: Digital WRL and Chandramohan A. Thekkath: Digital SRC*

An Integrated Compile-Time/Run-Time Software Distributed Shared Memory System, *Sandhya Dwarkadas, Alan L. Cox and Willy Zwaenepoel: Rice University*

Hiding Communication Latency and Coherence Overhead in Software DSMs, *R. Bianchini: Federal University of Rio de Janeiro, L. I. Kontothanassis: Digital CRL, R. Pinto, M. De Maria, M. Abud and C. L. Amorim: Federal University of Rio de Janeiro*

SoftFLASH: Analyzing the Performance of Clustered Distributed Virtual Shared Memory, *Andrew Erlichson: Stanford University, Neal Nuckolls, Greg Chesson: Silicon Graphics, Inc. and John Hennessy: Stanford University*