Reconfigurable Issue Logic for Microprocessor Power/Performance Throttling

Dave Maze
Edwin Olson
Andrew Menard

Observation

- Complex issue logic for out-of-order, speculative machines consumes a significant amount of power.
- Performance increase by complex issue logic is small.

Power/Performance Throttling

- Many applications have significant peak processing performance requirements but low average performance requirements.
- Very low power microprocessors can't deliver best of breed performance. Fastest uPs consume way too much power.
- Examples: handheld device which might be in standby, waiting for user input, MP3 player mode, or MPEG4 video playback

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What about Voltage/Frequency Scaling

- Reducing voltage (factor of α decreases performance by factor of α but decreases power consumption by α^2.)
- Voltage scaling runs out of steam as Vdd's approach a few Vt. Need other mechanisms for throttling power/performance.

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Why is Issue Logic so power hungry?

- In issue queue, every instruction is checked *every cycle* to see if it can be dispatched. This involves broadcasts of data on long bitlines.
- In 21264, queues compaction accounts for additional energy.
- Alpha 21264 consumes 18-46% of total energy in issue logic [Gowan] [Gupta].

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Our Three Approaches

- Add separate simple core to complex uP and switch between them
  - Mode switches slow. Only 2 performance points.
- Only use a subset of the issue window
  - Probably not as low-power. Provides continuum of performance points. Mode switches easy.
- Bypass issue logic completely
  - Must flush issue window. Only 2 performance points.

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Preliminary Results

	1x4 IO	2x4 IO	4x16 OO
IPC	0.57	0.64	1.39
Issue Power	1.75	2.06	6.12
Total Power	6.83	7.1	14.7
Issue Power %	25.6	29	41.6
IPC/Power	0.083	0.09	0.095
IPC/Issue Power	0.33	0.31	0.23

- Issue Width X Window Size X In/Out of Order
- Using identical technologies
- 1 issue is *very* poorly modeled; IPC is probably too low and power is almost certainly too high.
- SpecInt95 li benchmark

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Issue window throttling

	4x32	4x16	4x8	4x4
IPC	1.41	1.39	1.23	0.89
Issue Power	7.47	6.12	4.75	3.14
Total Power	16.83	14.71	12.4	9.28
Issue Power %	44.4	41.6	38.3	33.8
IPC/Power	0.084	0.094	0.099	0.096
IPC/Issue Power	0.032	0.033	0.032	0.026

Issue width x window size

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Tools

- Using Wattch (based on SimpleScalar) for high-level architectural modeling. Wattch gives us IPC and power data.
- Unable to measure critical path differences with Wattch. Open to suggestions… ??

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Plan

- Build better models of in-order processors to provide fairer comparison.
  - Custom tool?
- Try to get timing information (?)
- For checkpoint 2, paper mostly done except for some final data results.

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