Power and Performance Analysis of PDA Architectures

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I. Summary

As PDA technology becomes more prevalent, certain performance attributes become increasingly important and limiting. Especially important is a PDA's ability to perform a certain set of basic tasks at a high level. The other major consideration, due mainly to battery life limitations, is power consumption level. By analyzing the ability of various PDA architectures to perform various tasks and analyzing the power consumption footprint, we can begin to draw conclusions as to weaknesses and or limitations in the current PDA technology.

II. Project Plan

Our primary goal is to author a standard benchmark suite that we can apply across multiple architectures. The PDAs that we plan to examine include the Compaq Aero (MIPS), Compaq iPAQ (StrongArm), Casio Cassiopeia (MIPS), and the HP Jornada (SH3). The samples we will analyze will run the Windows CE operating system.

Current benchmarking suites focus on testing the optimization of processors to expediently perform specific tasks such as the ability to perform high speed arithmetic operations (such as large matrix multiplication). Current PDA usage trends would suggest that while the ability to perform these operations is necessary, they are overshadowed by the far more commonly used operations.

Consequently, we plan to target our test suite towards several common user interface needs which we have identified: the ability to quickly and seamlessly perform a context or task switch; the ability to quickly render GUI elements such as window forms, buttons, etc.; and the speed of performing handwriting recognition. We also plan on benchmarking several applications of PDAs, the use of which we foresee becoming more prevalent and important in the future. These would include rating the performance of java bytecode running in a PDA JVM, vs. the performance of the same code running on a known architecture, such as Sun/Solaris, etc. We also plan to look into multimedia applications such as MP3 and MPEG video decoding and playback.

We will run these benchmarks against our PDA samples while we measure power consumption. We plan to do this by placing a small resistor in series with the power supply line from the battery and measure and digitize a voltage reading across that resistor. We hope to be able to compare this digitized readout against the instruction code in our benchmark suite to isolate sequences that cause excessive power consumption.

III. Project Logistics

We plan to have the bulk of development on the test suite completed by the first checkpoint (Oct. 19), and fully completed shortly thereafter. Following that, we plan to collect power consumption data before the second checkpoint (Nov. 9) such that we may draw some primary conclusions. We plan to spend the last weeks drawing final conclusions about weaknesses or limitations in the technology and how they may be improved or solved in the future.

We plan to work on all components of this project jointly.