Cool Code Compression for Hot RISC

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Introduction

- Embedded processors make up half of the processor market
- Complexity of embedded systems has grown rapidly over the past several years
- Increase in size of embedded code contradicts goals of low cost and small area
- Code compression is a means of keeping code size from becoming too large
Code Compression Techniques

• Text compression provides basis for current techniques
  – Statistical compression
  – Dictionary compression
• Example systems
  – CCRP
  – Lefurgy97
  – CodePack
• Another alternative: modify the instruction set
  – Thumb
  – MIPS16

Our Proposal

• Examine code compression from the aspect of low power
• Select suitable compression algorithm
• Modify compiler to generate compression-friendly code
• Develop efficient hardware decompression scheme
Plan of Work

- Vanilla Pekoe is the target microprocessor
- gcc (egcs-1.0.3a) is the compiler
- SyChoSys will be used to simulate performance and energy
- Workload: SPECint95, SPECint2000, MediaBench
- Timeline
  - First project checkpoint
    • Compression algorithm selected
    • Initial compiler modification and hardware design
  - Second project checkpoint
    • Compiler support fully implemented
    • Working hardware decompression scheme