Investigating Predictive Techniques for Out of Order Logic

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The Problem

- Out of order logic is getting more complex, increasing power consumption.
- Optimized for performance, not power

- *How can memoization and predictive techniques be applied to introduce power savings?*

Methodology

- Examine key out of order logic structures:
  - Register renaming
  - Superscalar issue logic
- Look for correlation between state and asserted control signals
- Redesign logical structures to increase correlation
- Add new logical structures to apply predictive techniques to out of order logic

Issues

- How do we determine the power savings of our scheme?
- How do we detect mispredictions, and what kind of mispredictions are possible?
- How do we recover from mispredictions in the issue logic?