Correlation Between State and Control Signals in Out-of-order Issue Logic

Checkpoint 2: 11/21/00

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Status Update

• Highlights
  – Data for individual instruction consistency
  – Data for PC_Fetch vs. Issue Window consistency
  – Data for register renaming
  – Data for instruction repetition

• Lowlights
  – Hard to collect large pipetraces
  – Spent a lot of time rewriting tools to support larger pipetraces
    • Repetition of research
Renaming Results

![Bar chart showing renaming results for various benchmarks.]

- **Bar Chart Description:**
  - **X-axis:** Benchmark
  - **Y-axis:** Fraction
  - **Legend:**
    - Mapped to Original Mapping
    - Could Map to Original Mapping

- **Benchmarks:**
  - cc1
  - compress
  - go
  - jpegs
  - li
  - mesg
  - perl
  - vortex
Individual Instruction Consistency

![Bar chart showing individual instruction consistency for 'ijpeg2', 'm88ksim', and 'perl2' benchmarks. The chart compares overall consistency and latency to EX consistency.](image-url)
Fetch_PC vs. Issue Window Consistency

![Graph showing percentage accuracy for different benchmarks and prediction methods.](image)
The Road to the Finish Line

• Issue Oracle
  – Verify functionality
  – Collect data
  – Compare results against expected results (consistency data)
  – Test different oracle prediction rules

• Renaming
  – Collect data for forced renaming

• Consistency Data
  – Greater variety of traces