DSL Technology for Exascale Computing (D-TEC)

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Co-PIs and Institutions

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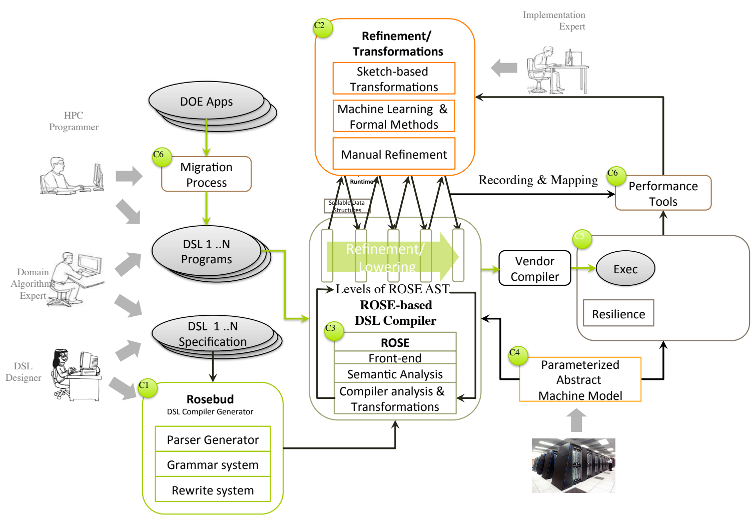
INTRODUCTION

- Domain Specific Languages define high level abstractions that make it efficient for the development of application code.
  - High-level abstractions improve productivity
  - Enables domain-specific performance and energy optimizations
- However, it is very difficult to efficiently leverage DSLs due to lengthy design and development of the corresponding software stack support, including languages, compilers, runtime and tools.

GOAL

Making DSLs effective for exascale
- Support both embedded and general (syntax extended) DSLs
- Address all layers of the exascale software stack: languages (DSLs), compilers, abstract machine, runtime, and tools
- Address multiple exascale challenges: scalability, programmability, performance portability, resilience, energy efficiency, correctness, and heterogeneity
- Include interoperability with MPI+X through translation to low level code
- Provide a migration strategy for legacy code through source-to-source technology

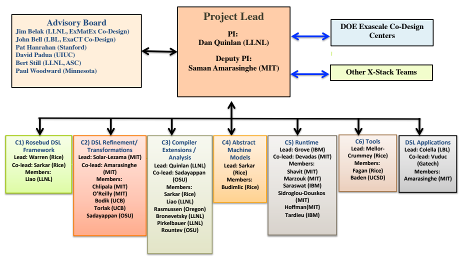
The D-TEC approach addresses the full Exascale workflow



APPROACH

- Languages (C1):
  - Discovery of domain specific abstractions through collaborative efforts from both computer scientists and application experts
  - Rosebud: define DSLs specification and plug-in
- Refinement/Transformation(C2):
  - Series of manual refinements steps (code rewrites) define the transformations
  - Equivalence checking between steps to verify correctness
  - Machine learning to drive optimizations
- Compiler (C3):
  - Leverage a source-to-source compiler infrastructure, ROSE, to create an DSL framework to support code rewriting, analysis and optimizations
- Parameterized Abstract Machine (C4): extraction of machine characteristics
- Runtime System (C5): leverages X10 and extends it with SEEC support
- Tools (C6): source-to-source migration tools and tools for mappings between DSL layers to support future tools

Management Organization Plan and Collaboration Paths with Advisory Board and Outside Community



Advisory Board
Jim Belak (LLNL, ExMatEx Co-Design)
John Bell (LBL, ExaCT Co-Design)
Pat Hanrahan (Stanford)
David Padua (UIUC)
Bert Still (LLNL, ASC)
Paul Woodward (Minnesota)
Project Lead
PI: Dan Quinlan (LLNL)
Deputy PI: Saman Amarasinghe (MIT)
DOE Exascale Co-Design Centers
Other X-Stack Teams
C1) Rosebud DSL Framework
Lead: Warren (Rice)
Co-lead: Sarkar (Rice)
Members: Liao (LLNL)
C2) DSL Refinement/ Transformations
Lead: Solar-Lezama (MIT)
Co-lead: Amarasinghe (MIT)
Members: Chlipala (MIT) O'Reilly (MIT) Bodik (UCB) Torlak (UCB) Sadayappan (OSU)
C3) Compiler Extensions / Analysis
Lead: Quinlan (LLNL)
Co-lead: Sadayappan (OSU)
Members: Sarkar (Rice) Liao (LLNL) Rasmussen (Oregon) Bronevetsky (LLNL) Pirkelbauer (LLNL) Rountev (OSU)
C4) Abstract Machine Models
Lead: Sarkar (Rice)
Members: Budimlic (Rice)
C5) Runtime
Lead: Grove (IBM)
Co-lead: Devadas (MIT)
Members: Shavit (MIT) Marzouk (MIT) Saraswat (IBM) Sidroglou-Douskos (MIT) Hoffman(MIT) Tardieu (IBM)
C6) Tools
Lead: Mellor-Crummey (Rice)
Members: Fagan (Rice) Baden (UCSD)
DSL Applications
Lead: Colella (LBL)
Co-lead: Vuduc (Gatech)
Members: Amarasinghe (MIT)

Summary

DSLs are expected to be a transformational technology to bridge the gap between diverse algorithms/applications and complex exascale machines. We are working on a comprehensive DSL framework to facilitate the definition, implementation and optimizations of DSLs for addressing multiple challenges arisen from the furture exascale computing. *More info at http://www.dtec-xstack.org.*

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